Design & Simulation of CMOS Inverter at Nanoscale beyond 22nm

Adil Zaidi, Kapil Garg, Ankit Verma, Ashish Raheja

Abstract — Power and area are the two major concerns in design of any digital circuit. At present scenario low power device design and its implementation have got a significant role in the field of nano electronics. This paper investigates the applications of CMOS technology in the nanometer regime beyond 22 nm channel length where the relative study of average power dissipation of CMOS inverter is found in nano Watts. The simulation results are taken at different channel length (16nm 22nm, 32nm, 45nm) using CMOS technology with the help of (H-spice) simulation tool. The results are analyzed at different supply voltages keeping constant load capacitance (C load =1fF) apart from this, values of various internal parameters of CMOS Inverter at different channel length are calculated.

Index Terms - Nano-electronics, UDSM (Ultra Deep Sub-Micron) Technology, CMOS, and Scaling.

I. INTRODUCTION

The increasing prominence of portable system and the need to limit power consumption in very high density VLSI chips has led to rapid and innovative development in low-power design for many years [1]. From the last few decades the CMOS technology has emerged as a predominant technology in the field of nano electronics. As the technology has become compact there is rapid increase in demand of high performance and low power digital systems. CMOS technologies rapidly captured the digital market CMOS gates dissipated power only during switching and required very few devices, two attributes in sharp contrast to their bipolar or GaAs counterparts. It was also soon discovered that the dimensions of MOS devices could be easily scaled down more easily than those of other types of transistors. Furthermore CMOS circuits proved to have a lower fabrication cost. CMOS technology is used due to the low cost of fabrication and possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance so as to reduce the cost of packaging [2].

Since the CMOS inverter does not draw any significant current form the power source in both of its steady state operating points, the DC power dissipation of the circuit is almost negligible. The drain current that flows through the nMOS and pMOS transistors in both cases is essentially limited to the reverse leakage current of the source and drain pn-junction [1].

The design of high density Chips in MOS VLSI technology requires that the packaging density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. Reduction of size i.e. the dimension of MOSFET gets reduced is termed as scaling [3]. With the help of scaling the electrical properties of the MOSFET can be altered and complexity is reduced [4]. Scaling seems to play a vital role in enhancing characteristic MOSFET which further leads to low power dissipation and cost per function.

Power consumption has repeatedly been the driving force behind changes in the preferred transistor technology of choice in designing integrated circuits (ICs). Moves from bipolar to nMOS and then nMOS to complementary MOS (CMOS) technologies occurred primarily due to the much lower power consumption [5]. To cope up with the limitations of power dissipation we scale down the dimensions of the transistor since the power delivered is proportional to the square of supply voltage VDD power dissipation occurs due to charging and discharging of load capacitance [6].

\[ P = C_L \cdot V_{DD}^2 \cdot F_D \]

Where

- \( P \) is the power dissipated,
- \( C_L \) is the load capacitance,
- \( V_{DD} \) is the power supply voltage and
- \( F_D \) is the frequency.

The advanced productions of integrated circuits are built on CMOS devices with minimum feature sizes of 40 nm. Here in this paper we are trying to design the CMOS inverter at channel length of 16nm starting from channel lengths 45nm, 32nm, 22nm using H-spice [7].

The paper is classified as follows: section II includes the design & power model of CMOS inverter at nano scale which describes the schematic view of the CMOS INVERTER considering its power dissipation factor. Section III describes simulated characteristics i.e. D.C and Transient curves at NANO SCALE. Section IV includes results and discussion. Section V contains acknowledgement followed by references in section VI.

II. DESIGN & POWER MODEL OF CMOS INVERTER AT NANO SCALE

![FIGURE 1. CMOS INVERTER]
A. DESIGN
MOSFETs are continuously scaled to smaller dimensions to reduce the space complexity. UDSM (Ultra Deep Sub-Micron) Technology deals with MOS devices with channel length in the order of 0.25μm to 0.022μm or even less. The integration of nanostructures at room temperature smaller than 10nm is far too sensitive to size variations of even a few atomic widths [8]. Here the CMOS inverter is designed at different nano scales as mentioned and the values of different parameters are also calculated as mentioned in the table 1. The CMOS inverter is shown in figure 1

B. POWER MODEL OF CMOS INVERTER
Three types of power dissipation occur in CMOS inverter circuits, which are given below:

(i) Leakage power Dissipation: In OFF-state, the main components of leakage currents are sub-threshold leakage (Isub), gate induced drain leakage (IGIDL), gate tunnelling leakage (IGATE) and band-to-band tunnelling (IBTBT).

(ii) Short-circuit Power: From the α-power law [9] the short circuit power dissipation model is

\[ P_{\text{short-circuit}} = \frac{1}{\alpha + \frac{1}{2}} \left( \frac{1 - 2v_T}{v_T} \right)^{\frac{\alpha+1}{\alpha}} \]

Where \[ v_T = \frac{V_{TH}}{V_{DD}} \]

III. DYNAMIC POWER OR SWITCHING POWER:
This type of power dissipation occurs due to the charging and discharging of load and parasitic capacitors. Dynamic power expression indicate that the average dynamic power of a complex gate due to the output load capacitance.

\[ P_{\text{dynamic}} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f + \sum_{i=1}^{n} \alpha_i \cdot C_i \cdot V_{DD} \cdot (V_{DD} - V_T) \]

Dynamic power expression indicate that the average dynamic power of a complex gate due to the output load capacitance [8].

Where,
- \( C_L \) = Load Capacitance,
- Vdd = Supply Voltage,
- f = Operating Clock Frequency and
- \( \alpha \rightarrow \) switching activity of gate (the probability of a 0-1 switch in a cycle)

Here in this paper we focussed to analyse the average dynamic power or switching power.

IV. SIMULATED CHARACTERISTICS
The dc and voltage transient characteristics as obtained for CMOS inverter using H-SPICE simulator tool at different channel lengths viz. 45nm, 32nm, 22nm, 16nm are shown below.

A. VOLTAGE-TRANSIENT CHARACTERISTICS

- Shows input voltage
- Shows output voltage
C. INTERNAL PARAMETERS

The various internal parameters mentioned in TABLE 1 are:

**Currents:** \( I_d, I_{bs}, I_{bd} \)

**Voltages:** \( V_{gs}, V_{ds}, V_{bs}, V_{th}, V_{od}, V_{dsat} \)

**Transconductances:** \( g_{ms}, g_{ds}, g_{mb} \)

**Capacitances:** \( C_{gd}, C_{gd}, C_{s}, C_{stot}, C_{dston}, C_{gs}, C_{dtot} \)

Other: Region of operation and Beta.

In the above parameters the various subscripts shown indicates:
- \( g \) for gate terminal
- \( d \) for drain terminal
- \( s \) for source terminal
- \( b \) for body or substrate
- \( t \) for total
- \( th \) for threshold
- \( o \) for output

**Parameters**

The parameters shown below are for different values of channel length viz. 45nm and 32nm.

<table>
<thead>
<tr>
<th>CHANNEL LENGTH</th>
<th>At 45nm</th>
<th>At 32nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PARAMETER</strong></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Region</td>
<td>Cutoff</td>
<td>Linear</td>
</tr>
<tr>
<td>( I_d )</td>
<td>-3.0736p</td>
<td>6.1367p</td>
</tr>
<tr>
<td>( I_{bs} )</td>
<td>-1.1000p</td>
<td>4.58e-20</td>
</tr>
<tr>
<td>( I_{bd} )</td>
<td>1.433e-24</td>
<td>-6.663e-26</td>
</tr>
<tr>
<td>( V_{gs} )</td>
<td>-1.1000</td>
<td>-1.1000</td>
</tr>
<tr>
<td>( V_{ds} )</td>
<td>-1.1000</td>
<td>45.8505n</td>
</tr>
<tr>
<td>( V_{bs} )</td>
<td>-1.1000</td>
<td>45.8505n</td>
</tr>
<tr>
<td>( V_{bd} )</td>
<td>555.2204m</td>
<td>-587.69m</td>
</tr>
<tr>
<td>( V_{dsat} )</td>
<td>41.5588m</td>
<td>-378.97m</td>
</tr>
<tr>
<td>( V_{od} )</td>
<td>-1.6552</td>
<td>-512.30m</td>
</tr>
<tr>
<td><strong>Beta</strong></td>
<td>1.5772m</td>
<td>359.213u</td>
</tr>
</tbody>
</table>

**TABLE 1:** VALUES AT 45nm & 32nm

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>At 22nm</th>
<th>At 16nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>( g_m )</td>
<td>82.0249p</td>
<td>7.5330p</td>
</tr>
<tr>
<td>( g_{ds} )</td>
<td>5.5889p</td>
<td>133.840u</td>
</tr>
<tr>
<td>( g_{mb} )</td>
<td>24.0493p</td>
<td>2.3834p</td>
</tr>
<tr>
<td>( C_{dston} )</td>
<td>117.3034a</td>
<td>151.079a</td>
</tr>
<tr>
<td>( C_{gd} )</td>
<td>111.4480a</td>
<td>233.366a</td>
</tr>
<tr>
<td>( C_{gs} )</td>
<td>116.3603a</td>
<td>259.622a</td>
</tr>
<tr>
<td>( C_{dtot} )</td>
<td>181.5563a</td>
<td>199.240a</td>
</tr>
<tr>
<td>( C_{g} )</td>
<td>31.8388a</td>
<td>103.563a</td>
</tr>
<tr>
<td>( C_{gpd} )</td>
<td>49.9393a</td>
<td>127.6948a</td>
</tr>
</tbody>
</table>

**FIGURE 3(c):** FOR 22nm

**FIGURE 3(d):** FOR 16nm
TABLE2: VALUES AT 22nm & 16nm

V. RESULTS & DISCUSSIONS

The simulated dc and ac characteristics shown in FIGURE 2 & 3 depicts the variation of input voltage with respect to output voltage and variation of output voltage with respect to time (time domain approach) respectively which help us to find out the average power dissipated at various channel length maintaining the different power supply as mentioned in the TABLE 3

<table>
<thead>
<tr>
<th>Channel Length (nm)</th>
<th>Optimum Supply Voltage (volts)</th>
<th>Power dissipation (Nanowatts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>1.1</td>
<td>398</td>
</tr>
<tr>
<td>32</td>
<td>0.95</td>
<td>241.6</td>
</tr>
<tr>
<td>22</td>
<td>0.9</td>
<td>238</td>
</tr>
<tr>
<td>16</td>
<td>0.8</td>
<td>215</td>
</tr>
</tbody>
</table>

TABLE3: AVERAGE POWER DISSIPATED WITH CHANNEL LENGTH

The figure 4 shows the variation of average power dissipated with respect to the channel length in nano scale based on the values mentioned in TABLE3. The graph clearly shows as the channel length is decreasing following the sequence, 45 nm, 32 nm, 22nm & 16 nm, the average power dissipated is also decreasing following an exponentially decaying curve thus the components density can be increased in a small area with an effective decrease in average power dissipation .Finally the CMOS inverter is designed at a nano scale of channel length 16nm with power supply of 0.8 volts will improve the power dissipation factor. Further the values of various internal parameters are presented in TABLE 1 & 2.

VI. ACKNOWLEDGEMENT

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