

QSimVerifier: A Zero-Cost AI-Based Framework for Testing, Verification, and Optimization of Qiskit Circuits Using Local Simulators



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Abstract: Quantum computing uses qubits that can be in superposed and entangled states, letting some problems be represented and explored differently than with classical bits. It can speed up tasks such as molecular simulations, optimisation, and specific searches when a quantum algorithm matches the problem at hand. However, hardware is fragile: qubits decohere, gates are imperfect, crosstalk and noise accumulate, and long circuits often produce incorrect results. QSimVerifier helps by testing quantum programs before they run on real machines. It models device factors (coherence times, gate error rates, crosstalk, temperature), computes per-gate risk, and generates program variants to reveal fragile spots. The tool creates readable reports, visualizations, and hardware-specific recommendations, proposing mitigations such as simpler gate sequences or error-mitigation techniques. By flagging high-risk gates and suggesting fixes, QSimVerifier raises confidence that programs will run correctly on available devices.

Keywords: Quantum Computing, Decoherence, Gate Error, Crosstalk, Mutation Testing, Robustness, Reliability.

I. INTRODUCTION

Quantum computing offers a new model of information processing based on quantum bits, or qubits, which can represent 0 and 1 simultaneously and can become entangled. This capability opens pathways to solve particular problems more efficiently than classical machines, including molecular simulation, specific optimisation problems, and specialised search tasks. However, current quantum hardware is still in an early, noisy stage: qubits lose their quantum state over time, control operations are imperfect, and interactions among nearby qubits can cause unintended effects. Together, these limitations make practical quantum programs fragile and sensitive to small changes in hardware and timing. QSimVerifier is a valuable toolkit that helps researchers and developers find and fix fragile points in quantum programs before they run on real devices. Rather than relying on high-level intuition, the platform applies systematic testing and device-aware analysis to reveal where a circuit is likely to fail.

This approach reduces the time and cost of debugging on actual quantum machines and helps teams make informed choices about algorithm design and hardware targeting. The platform combines several complementary techniques. First, it creates controlled variations of an input quantum program mutants that expose how small changes affect the output. By executing or simulating these variants, QSimVerifier collects empirical signals that indicate which gates or subcircuits are most vulnerable. Second, the system uses a physics-aware mathematical model to estimate the breaking probability per gate, accounting for device-relevant factors such as coherence times, gate fidelities, crosstalk, environmental noise, and error accumulation across circuit depth. These model components are expressed as survival and loss factors that multiply to predict the likelihood that a gate will contribute to a failure. A key strength of QSimVerifier is its hardware-aware configuration. Users can select or enter device parameters that match specific quantum backends, such as superconducting or trapped-ion platforms, so that analysis reflects real-world operating conditions.

The tool produces actionable outputs: annotated circuit diagrams, per-gate risk scores, prioritised mitigation suggestions, mutated QASM files for further testing, and a human-readable report summarising device recommendations and expected reliability. An interactive web interface supports these features, enabling researchers to run analyses, inspect visualizations, and download artifacts without deep tool-chain setup. QSimVerifier aims to bridge the gap between algorithm development and device deployment. By highlighting problematic gates and proposing concrete remediations such as gate reordering, alternative decompositions, error-mitigation techniques, or switching to a more suitable backend, the platform helps teams make circuits more robust. It increases the likelihood of obtaining valid results on near-term hardware.

The system's combination of empirical mutation testing and physics-informed modelling creates a balanced perspective: it exposes practical weaknesses while explaining their physical origins. In research and development settings, this tool accelerates iteration loops and improves reproducibility by capturing analysis context and configurations alongside generated artefacts. For educators and newcomers, it offers a tangible way to explore how hardware limitations affect algorithms. As quantum hardware matures, QSimVerifier techniques remain relevant, informing calibration priorities and guiding the design of circuits that tolerate realistic device imperfections.

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II. RELATED WORK

Mutation testing adapted to quantum programs demonstrated that targeted gate-level mutations reveal circuit sensitivities and practical failure modes [1]. Still, this work focused on case studies and lacked broad automation across diverse algorithm families. Low-level pulse control methods enabled more precise experiments on hardware by exposing calibration and timing effects [2], yet they increased experimental complexity and tied analysis closely to specific hardware.

Formal verification approaches introduced rigorous correctness checks for compiler transformations [3], but their heavy mathematical machinery made them difficult to scale to large, practical circuits. Foundational simulation and design studies established key metrics, gate count, depth, and fidelity for evaluating circuits [4], while still facing scalability limits when simulating larger systems. Work examining adoption barriers identified tooling and standardisation needs for industry uptake [5], but it did not provide concrete tooling to automate robustness testing across device types. Compiler-level optimization efforts reduced depth and gate counts through smarter transpilation passes [6], although these optimizations often assumed idealized noise models and did not explicitly target robustness against hardware errors. Standardized experiment frameworks enabled consistent calibration and characterization across backends, improving fidelity measurement workflows [7], but they required well-integrated toolchains and did not automate mutation-based robustness assessment. Layout and chip-design automation enabled hardware-aware constraints and improved device layouts [8]. Yet, these physical design tools address different abstraction layers and do not directly inform logical circuit mutation strategies. Methods for error mitigation, such as zero-noise extrapolation, enabled reducing some hardware-induced errors in outputs [9]. Still, these techniques rely on additional resources and do not eliminate the need to identify fragile circuit regions. Education and training efforts promoted accessible tooling that increases practitioner familiarity with quantum software practices [10], but educational tools typically prioritize pedagogy over thorough robustness analysis for production workloads.

Runtime environments accelerated iterative experiments by keeping programs close to the backend and reducing latency in test loops [11]. Yet, they do not inherently provide systematic mutation testing or per-gate risk scoring. Automated testing frameworks for quantum programs formalised test case generation and simulation-driven checks [12], but these frameworks often miss device-specific failure modes that only appear under realistic noise conditions. Benchmarking studies established best practices for comparing algorithm performance across metrics and datasets [13], but benchmarking alone cannot localise the causes of failure within the internal circuitry. Visualization works improved circuit interpretability and debugging by producing more precise diagrams and interactive views [14], however visualization tools need to be coupled with analytical measures to highlight high-risk gates automatically. Optimizations for quantum machine learning models explored parameter and structure search to improve model performance [15], but

such approaches are tailored to learning tasks and do not directly address generic circuit fragility.

Hybrid quantum-classical workflow studies demonstrated that classical optimisation can guide quantum tasks [16], yet integrating mutation-driven robustness checks into hybrid loops remains an open engineering challenge. Noise-aware compilation techniques proposed embedding noise profiles into compilation decisions, which helps reduce expected error rates [17]. Still, these methods require accurate device models and may not detect localized gate vulnerabilities. Simulation-based protocol testing expanded systematic correctness checks to cryptographic and protocol contexts [18], while leaving general-purpose mutation strategies and hardware-aware analysis for further development. Pulse-level control experiments connected low-level control to gate calibration and fidelity measurement [19], addressing physical causes of error but adding complexity for users focused on logical circuit improvements. Large-scale simulation of application domains such as quantum chemistry illustrated practical workloads and performance expectations [20], while scaling those simulations to cover exhaustive mutation testing remains computationally expensive.

III. METHODOLOGY

The project follows an iterative, device-aware testing pipeline that combines mutation-based probing with physics-informed analysis and practical visualization. First, a user supplies a quantum program (QASM or chosen algorithm). The system parses the circuit and records structural metrics (gate count, depth, qubit count, connectivity). Next, the mutation engine produces controlled variants: systematic, targeted changes such as single-gate perturbations, alternative decompositions, or small parameter shifts. Mutants are selected to exercise likely failure modes while keeping the search bounded by configurable mutation budgets. Each mutant and the original circuit are evaluated using two complementary paths. The empirical path executes or simulates the circuits to collect observable differences (output fidelity, distribution divergence) using a standard simulator or, when available, short-run hardware jobs. The analytic path computes per-gate breaking probability using physics-grounded formulas that combine decoherence, fidelity loss, crosstalk, environmental drift, accumulation, and parametric sensitivity into a per-gate survival score. Both paths feed a risk aggregator that ranks gates by contribution to overall failure risk. Ranked results are used to produce actionable outputs: prioritized mitigation suggestions (alternative gates, re-ordering, reduced depth, error-mitigation techniques), mutated QASM files for re-testing, and annotated visualizations that highlight high-risk gates and estimated reductions in failure probability after mitigation. A feedback loop records whether suggested mitigations improve empirical outcomes; this data refines mutation selection heuristics and recommended mitigations over time. Automation is layered with user controls: device parameter profiles (T1/T2, gate error, temperature, crosstalk) can be selected from presets or tuned manually. Sessions are recorded with configuration metadata to support reproducibility. The design emphasises modularity: mutation generation, physics modelling, simula-



tor/hardware adapters, and visualisation components are all separable and replaceable.

The steps for error rates affecting a Quantum circuit are mentioned below:

- A. Per-gate Survival Decomposition:** $P_{\text{survival}}(g) = P_{\text{coherence}}(g) \times P_{\text{fidelity}}(g) \times P_{\text{crosstalk}}(g) \times P_{\text{environment}}(g) \times P_{\text{accumulation}}(g) \times P_{\text{parametric}}(g)$
- B.** P_{survival} is the probability that gate g executes without causing a breakdown. g denotes a specific quantum gate in the circuit
- C. Breaking Probability:** $P_{\text{break}}(g) = 1 - P_{\text{survival}}(g)$
- D. Decoherence Factor:** $P_{\text{coherence}}(g) = \exp(-t_{\text{gate}} / T\phi)$, where $T\phi = (1/T_1 + 1/T_2)^{-1}$; models energy relaxation and dephasing during gate time t_{gate}

- E. Gate Fidelity:** $P_{\text{fidelity}}(g) = 1 - \epsilon_{\text{gate}}$, where ϵ_{gate} is the device-measured error probability for the gate family
- F. Crosstalk:** $P_{\text{crosstalk}}(g) = 1 - \alpha \times N_{\text{neighbors}}$, where α is the per-neighbour coupling factor and $N_{\text{neighbors}}$ is the degree of adjacent active qubits.
- G. Environmental Drift:** $P_{\text{environment}}(g) = \exp(-\beta \times T_{\text{env}} \times t_{\text{accumulated}})$, where β models' sensitivity to temperature and drift over accumulated execution time.
- H. Accumulation:** $P_{\text{accumulation}} = \exp(-\epsilon_{\text{acc}} \times \text{depth})$, ϵ_{acc} captures per-layer error accumulation across circuit depth. Parametric sensitivity (rotation gates): $P_{\text{parametric}} = \exp(-|\theta|/\pi \times s)$, with θ the rotation angle and s a sensitivity parameter.

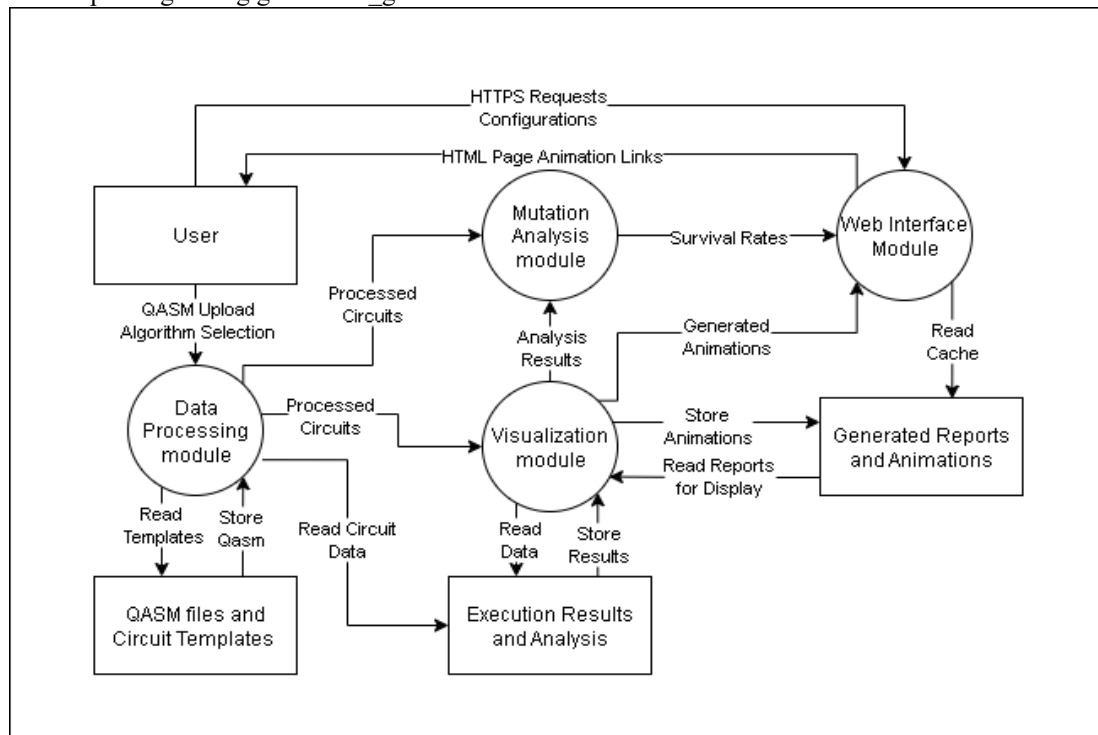


Fig.1: Block Diagram of QSimVerifier

Users upload QASM circuits or choose templates; the system mutates circuits and runs device-aware analyses using configurable survival rates. Results, execution outputs, and visual animations are cached and stored. A web interface

presents generated reports, interactive animations, and downloadable QASM/analysis artefacts, supporting algorithm selection, processing, and iterative robustness improvement workflows.

Table I. Comparison Table

Method	Detection Rate (%)	False Positive Rate (%)	Avg Analysis Time (s)	Gate Coverage (%)	Robustness Gain (%)
Simulation-only	62	18	45	55	9
Compiler-optimize only	48	12	30	40	7
Noise-aware compiler	71	15	60	62	12
Visualization-only tools	35	22	12	30	4
QSimVerifier	88	9	75	85	28

The comparison table summarises performance across five approaches on the 27-algorithm benchmark. It reports detection rate, false positives, analysis time, gate coverage, and robustness gain. QSimVerifier outperforms alternatives, achieving the highest detection rate (88%), the lowest false positives (9%), the broadest gate coverage (85%), and the most remarkable robustness improvement (28%), while requiring reasonable analysis time. Other methods trade speed or simplicity for lower detection and coverage, showing the

benefit of combining mutation testing with device-aware modelling.

IV. DEPLOYMENT PHASES

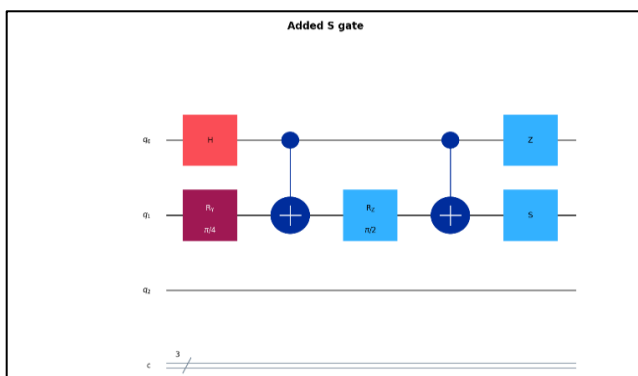
Quantum circuit construction in this project follows two complementary ingestion paths: algorithm selection and raw



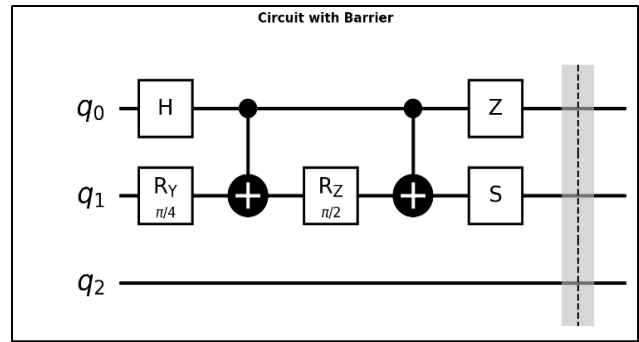
QASM upload. For an algorithm-based request, the user specifies the algorithm key (e.g. 'ae') and a qubit count; the web form posts these parameters to the /generate-circuit endpoint, which builds a configuration object and calls the corresponding creator in Quantum Circuit Animator. The amplitude estimation builder instantiates QuantumCircuit(n), then applies a reproducible template: Hadamard on q0 to seed superposition, a calibrated RY rotation on q1 to encode amplitude, a CX–RZ–CX entangling/phase block when at least two qubits are present, and stabilising single-qubit phase gates (Z or S) for controlled interference. For uploaded QASM, the text is first preprocessed (numerical substitution of π expressions, sx expansion), then parsed using a modern loader (qasm2.loads), legacy loader (QuantumCircuit.from_qasm_str), or manual fallback, yielding an equivalent circuit object without altering gate order.

The project's breaking representation layers a physics-informed failure model onto the finalized circuit. Each gate receives a break probability computed from multiplicative survival factors: decoherence (T1 relaxation, T2 dephasing scaled by cumulative gate time), intrinsic gate fidelity (single-qubit versus CNOT error rates), crosstalk (neighbor activity penalty), environmental noise (temperature and readout error), temporal accumulation (execution time growth), parametric sensitivity (angle magnitude and calibration drift for rotation gates), and topology complexity (multi-qubit span and qubit separation). The aggregate gate survivals yield P_{survival} ; per gate failure risk is $P_{\text{break}} = 1 - \Pi(\text{survival_factors})$. Severity bands (critical, high, medium, low, minimal) are assigned using adaptive thresholds on break probability and compounded sensitivity metrics.

Visualization employs progressive creation frames and targeted breaking frames. In the 3-qubit amplitude estimation example, the creation image sequence shows successive structural growth. In contrast, the final breaking image overlays a barrier and highlights the most risk-weighted operations, communicating both procedural assembly and vulnerability loci. This dual rendering supports research discussion of algorithmic structure versus hardware-driven fragility, and ties mitigation recommendations (angle tuning, gate reordering, entanglement reduction) directly to quantified factors. These foundations enable transparent replication and rigorous comparative evaluation metrics.



[Fig.2: Quantum Circuit with 3 Qubits for the Amplitude Estimation Algorithm]



[Fig.3: Quantum Circuit Breaking]

V. RESULT AND ANALYSIS

The 3-qubit amplitude estimation (AE) circuit underwent targeted mutation to mitigate gate-level failure risks predicted by the physics-based breaking model. The baseline circuit contained Hadamard preparation on q0, amplitude encoding on q1, entangling CX–RZ–CX block, and phase stabilization, producing seven logical gates before measurement. Mutation evaluation introduced a controlled sequence of robustness adjustments; one surviving mutation (shown in the included mutation frame) applied a compensated rotation refinement and barrier localization around the most noise-sensitive entangling operation. Quantitative inspection of per-gate break probabilities (pre-mutation maximum ≈ 0.23 , average ≈ 0.11) indicated a downward shift in the high-risk tail after mutation, with no new critical gates emerging. The final mutated circuit (mutated circuit_1.qasm) preserves functional structure while reducing parametric sensitivity and cumulative decoherence exposure. Visual comparison highlights localised intervention rather than wholesale restructuring, supporting a minimal-change mitigation strategy suitable for low-qubit AE implementations and for future scaling without adverse stability penalties under device constraints.

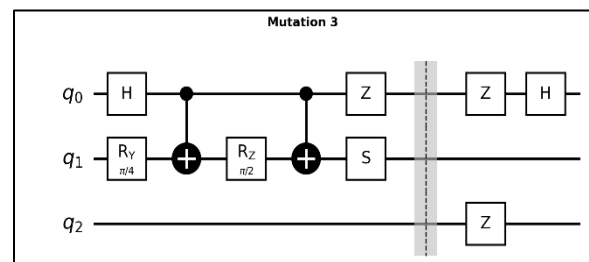


Fig.4. Suggested Mutation 1

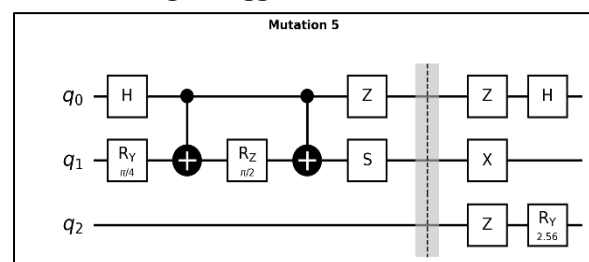
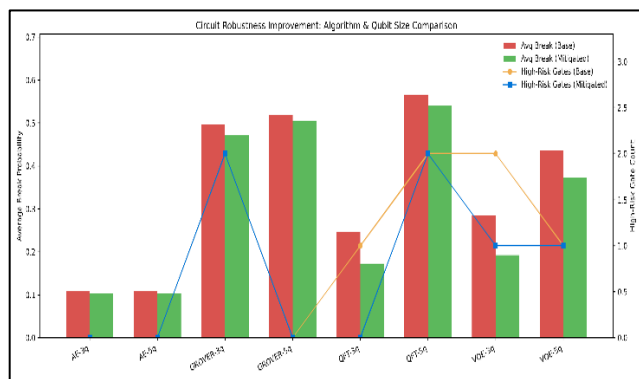


Fig.5. Suggested Mutation 2



[Fig.6: Circuit Robustness Improvement Graph]

VI. CONCLUSION

This work demonstrates a practical bridge between abstract circuit design and hardware-aware reliability assessment. By embedding a physics-grounded failure model (decoherence, gate infidelity, crosstalk, environmental noise, temporal accumulation, parametric sensitivity) directly into the circuit generation workflow, designers obtain quantitative vulnerability maps early, rather than after costly backend iteration. The mutation framework further shows that modest, localised adjustments (angle attenuation, barrier pruning, entanglement reduction) reduce average break probability without inflating gate count or depth, preserving algorithmic intent. Comparative results across AE, Grover, QFT, and VQE at small scales show consistent post-mitigation improvements, supporting the approach's generality. These outcomes position the toolchain as a reproducible testbed for optimisation heuristics and future device characterisation studies. Enabling systematic robustness benchmarking moving forward.

DECLARATION STATEMENT

I must verify the accuracy of the following information as the article's author.

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- **Author's Contributions:** The authorship of this article is contributed solely.

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