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Design Low Power Full-Adders for Arithmetic Applications

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Abstract-This paper presents low power CMOS full adder cells. The full adder cells are utilization to low power by using XOR and XNOR gate architectures with pass transistor logic and transmission gate. All simulation results have been carried out by using HSPICE program simulator based on 22 nm CMOS technology at 1.2 V supply voltages. The operating frequency is 250 MHz. In comparison with other 1 bit adder cells, simulation results show that have used low power consumption and power delay product of SUM and C_{OUT}.

Index Terms—A CMOS full adder, XNOR-XOR gate, low power full adder.

I. INTRODUCTION

In very large scale integration (VLSI) systems, full adder circuit is used in arithmetic operations for addition, multipliers and Arithmetic Logic Unit (ALU). It is a building block of the application of VLSI, digital signal processing, image processing and microprocessors. Most of full adder systems are considered performance of circuits, number of transistor, speed of circuit, chip area, threshold loss and full swing output and the most important is power consumption. In the future, portable devices such as cell phone, laptop computer, tablet etc. that need a low power and high speed for components are requirements. For this reason, design of low power is the research problems. In the paper is proposed I-bit full adder base on 22 nm CMOS technology which operation for low supply voltage is 1.2V at 250 MHz.

II. PREVIOS WORKS

Full adder circuit is designed for addition binary logics.

Sum signal (SUM) and carry out signal (COUT) are the output of I-bit full adder. Both of them are generated by input A, B and C_{IN}, following Boolean equation as:

$$SUM = A \oplus B \oplus C_{IN} \quad (1)$$

$$C_{OUT} = AB + BC_{IN} + AC_{IN} \quad (2)$$

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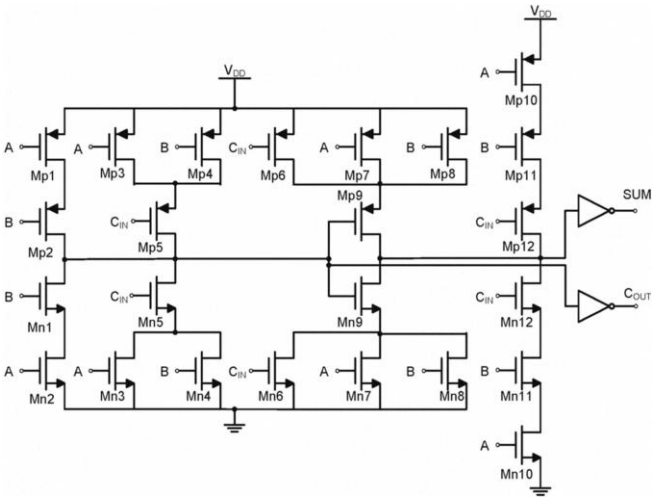

Figure 1. Conventional CMOS full adder [1]-[4]

Conventional CMOS full adder [1]-[4], as shown in Fig. 1, is the complementary CMOS structure, which combines transistor PMOS pull-up and transistor NMOS pull-down network to produce output. The complementary CMOS logic circuit has the advantage of layout regularity and stability at low voltage. It has a high transistor count which consumes area and power. The problem of this adder is delay imbalance. Because SUM signal relies on the generation of COUT signal, there is a delay between two signals. The transmission gate full adder is illustrated in Fig. 2, which based on transmission gate [5]. It has lower-transistor count and lower loading of the input. After generated, SUM and COUT signal are balanced than the Conventional CMOS full adder. It provides transistor buffer output of SUM and COUT for a high driving capability. In Fig. 3 shows the hybrid logic full adder [6]. It improves performance of speed and driving capability. A weak point of this circuit is separating between SUM and COUT circuits.

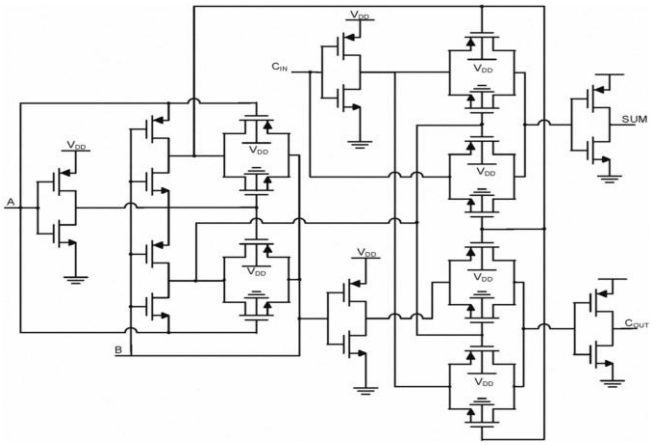

Figure2. Transmission gate full adder [5]

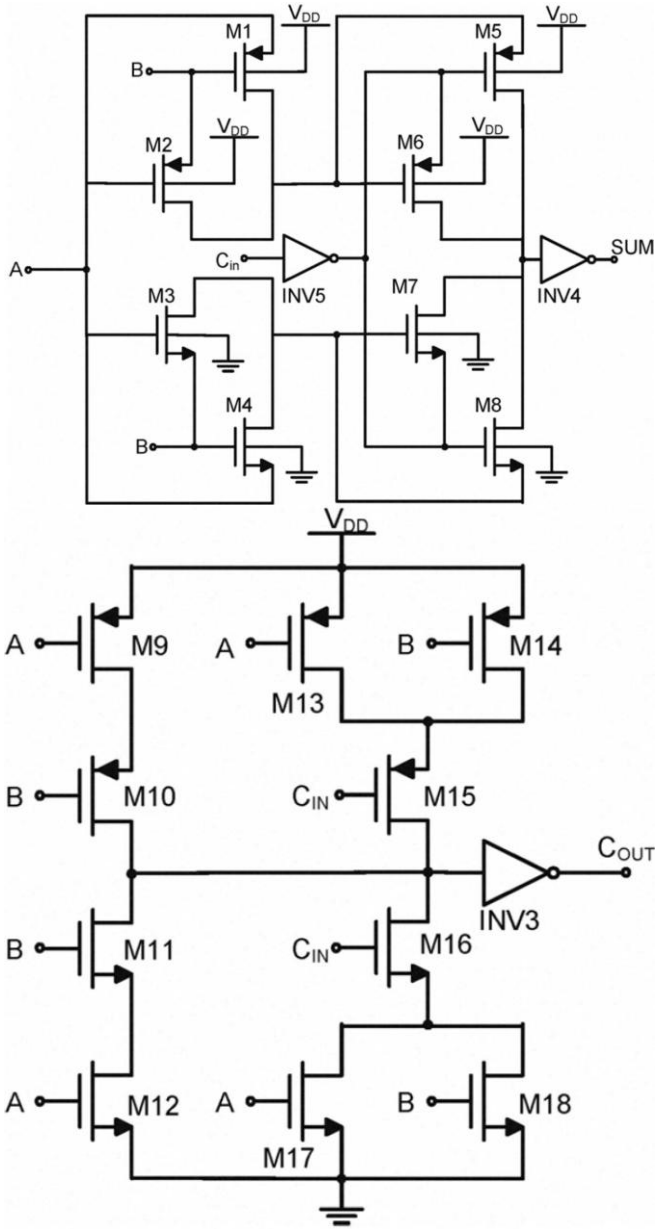

Figure3. Hybrid logic Full adder [6]

In Fig.4 shows Hybrid transmission gate/pass transistor logic full adder [7]. It is developed from transmission gate, pass transistor logic and enhance the driving capability by insert inverters at output. Its drawback is high power consumption.

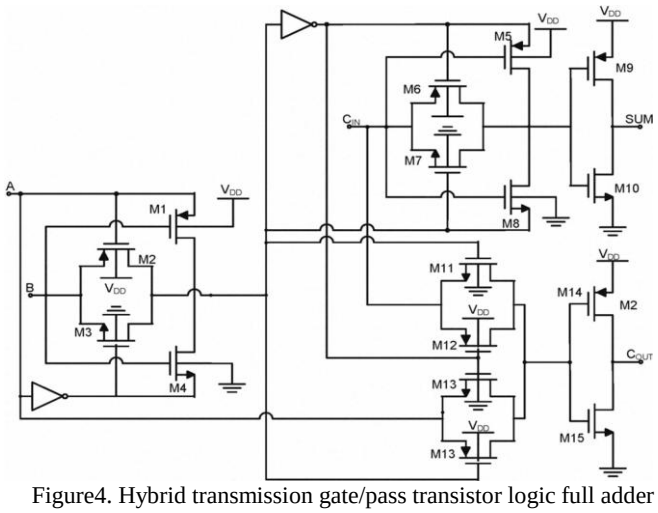

Figure4. Hybrid transmission gate/pass transistor logic full adder [7]

III. PROPOSED CIRCUIT

The proposed circuit is used pass transistor logic and transmission gate as shown in Fig.5. It has been developed for low power consumption by reducing the number of transistor. By applying the multiplexor into the proposed circuit and using inverter to increase the ability to drive. It follows Boolean equation as:

$$SUM = (A \overline{\oplus} B)C_{IN} + (A \oplus B)C_{IN} \quad (3)$$

$$C_{OUT} = \left(A(A \overline{\oplus} B)\right) + \left(C_{IN}(A \oplus B)\right) \quad (4)$$

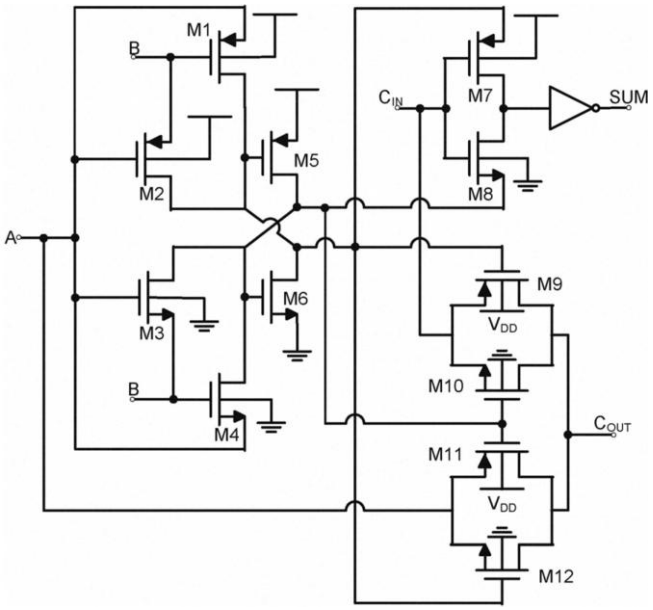

Figure5. Proposed full adder circuit

The operation of the proposed circuit is separated to 3 modules. The ftrst modules will generate function XOR and XNOR by using transistors MI-M6. It is pass transistor logic with cross-coupled CMOS to reduce the threshold voltage loss. This part has 2 inputs are A and B. When A=1 and B=1 then transistors M 1-M4 are tum off. The output for feedback drive from transistor M5 is equal 0 and transistor M6 is equal I. When the input switching, the input A is hold state and 8 = O. Transistors M 1 and M3 are tum on then transistors M5 and M6 are tum off that the output of transistor M1 is 1 and transistor M3 is O. When A=1, B=1 then transistors M1 and M3 are tum off and transistors M2 and M4 are tum on. The output of transistor M2 is 1 and transistor M4 is 0. Finally, when switching input, A=0 and B=0, transistors M2 and M4 are tum off. The outputs are generated by cross couple comparative with case A=I and 8=\. The second module is involved to the creation of SUM signal, following as equation (3). It is CMOS multiplexor by using transistors M7 and M8. The operation of this module when CIN =0, transistor M7 is tum on then the output is XNOR logic. When CIN=1, transistor M8 is tum on and transistor M7 is tum off then the output is XOR logic. The finally module, It is the transmission gate circuits. This module is used transistors M9-M12 to generate COUT signal, following as equation (4).

IV. SIMULATION RESULTS AND COMPARISON

To demonstrate the performance, simulation environment as shown in Fig. 6, Two CMOS inverters are added in the input and output node to predict the performance of circuits. It provides a situation similar realistic condition where the cell has driving circuit and driven circuit. The HSPICE simulations have been performed on these adders base on 22 nm CMOS technology at 1.5V power supply. The operating frequency is 250 MHz. The simulation results have been compiled into Table I

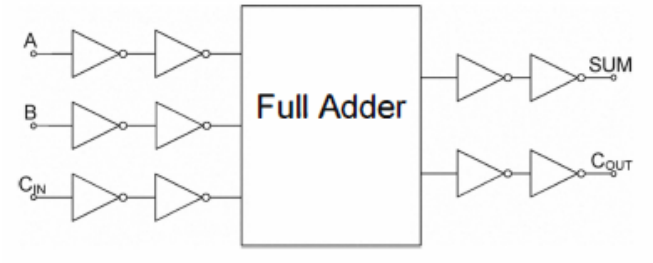

Figure 6. Simulation environment

The input/output buffers are included in the simulation. The delay time had been measured from the time at input reach 0% of voltage supply level to the time at the latest of the SUM and C_{OUT} signal reach to the same voltage level. The maximum delay of all the transitions is the cell delay. In measurement of power consumption of circuit, environment's inverters are excluded in calculation power. The output waveforms of the proposed full adder circuits are showed in Fig.7.

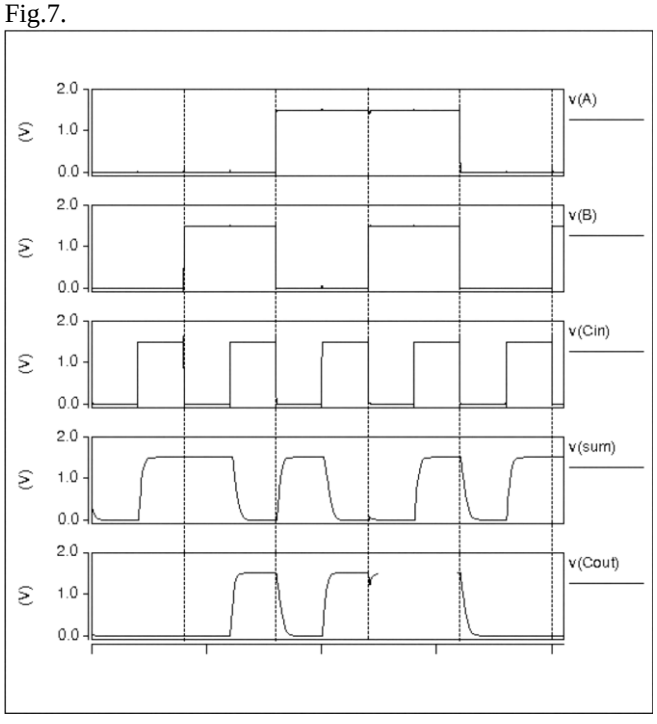

Figure7. Waveform of the proposed circuit at supply voltage I.5V

Power-delay product (PDP) is the important standard parameter for CMOS circuits. This value is calculated from power consumption multiplied with time delay. In Table I show the power consumption of the proposed circuit decreases to be 35.35%, 16.57% 30.38% and 34.80% when compared with CCMOS circuit, TGA circuit, HLFA circuit and Ref. [4] circuit, respectively.

TABLE I. SIMULATION RESULT FOR FULL ADDER

Full adder (V_{DD}=1.5v)	#tr.	Pd(uW)	Td(ns)		PDP (uW×nS)	
			SUM	C_{OUT}	*SUM*	C_{OUT}
CCMOS[1]	28	24.5	0.19	0.18	4.655	4.483
TGA[2]	26	21.1	0.19	0.18	4.072	3.798
HLFA[3]	24	23.6	0.38	0.17	9.109	4.130
Ref.[4]	20	24.4	0.23	0.17	5.735	4.318
Proposed	14	18.1	0.22	0.16	4.054	2.896

The power-delay product of SUM of proposed circuit is 14.82%, 0.44%, 124.69% and 41.46% for CCMOS circuit, TGA circuit, HLFA circuit and Ref. [4] circuit, respectively. The power-delay product of COUl of the proposed circuit is 54.79%, 31.14%, 42.61% and 49.10% for CCMOS circuit, TGA circuit, HLFA circuit and Ref. [4] circuit, respectively.

In Fig.8 shows the waveform of the proposed circuit which operates in 1.2V supply voltage at 250MHz. The simulation result, this proposed consumes the power of 12.6 IlW. Power delay product of sum is 7.64 pJ and power-delay product of
COUT is 2.76 pJ.

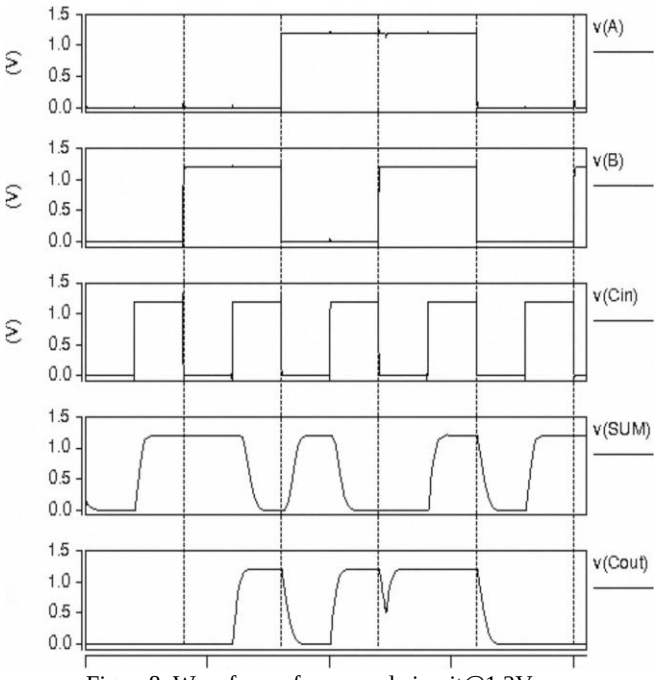

Figure8. Waveform of proposed circuit@1.2V

V. CONCLUSION

The low power 1- bit full adder circuit is proposed, it is suitable for using with 1.2 voltage supply voltage level at 250 MHz. The proposed circuit uses 14 transistors for complete operation; it has the power consumption less than CCMOS circuit, TGA circuit, HLFA circuit and Ref. [4] circuit. Moreover, the power-delay product term of SUM and COUT are lower than overall previous circuits. The HSpice program

simulator is used to carry out the signal at various terminals.

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