Performance Analysis of Three-Phase Three-Leg AC/AC Converter using SPWM and SVPWM

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***Abstract*—This paper proposes a three-phase nine switch ac/ac converter topology. This converter features sinusoidal inputs and outputs, unity input power factor, and more importantly, low manufacturing cost due to its reduced number of active switches.. . A suitable pulse width modulation (PWM) technique is employed to obtain the required output voltage. The different methods for PWM generation can be broadly classified into Triangle comparison based PWM (TCPWM) and Space Vector based PWM (SVPWM).**

In TCPWM methods such as sine-triangle PWM, three phase reference modulating signals are compared against a common triangular carrier to generate the PWM signals for the three phases. In SVPWM methods, a revolving reference voltage vector is provided as voltage reference instead of three phase modulating waves. The magnitude and frequency of the fundamental component in the line side are controlled by the magnitude and frequency, respectively, of the reference vector. The highest possible peak phase fundamental is very less in sine triangle PWM when compared with space vector PWM. Space Vector Modulation (SVM) Technique has become the important PWM technique for three phase AC-AC converters for the control of AC Induction, Brushless DC, Switched Reluctance and Permanent Magnet Synchronous Motors.

The study of space vector modulation technique reveals that space vector modulation technique utilizes DC bus voltage more efficiently and generates less harmonic distortion when compared with Sinusoidal PWM (SPWM) technique. In this paper first a model for Space vector PWM is made and simulated using MATLAB/SIMULINK software and its performance is compared with Sinusoidal PWM. The simulation study reveals that Space vector PWM utilizes dc bus voltage more effectively and generates less THD when compared with sine PWM.

***Index Terms*—AC/AC converter, pulse width modulation (PWM), reduced switch count topology**

I. INTRODUCTION

Three-Phase ac/dc/ac and ac/ac converters with variable frequency (VF) and variable voltage operation have found wide applications in the industry. The most popular configuration uses voltage source inverter (VSI) with a diode rectifier as the front end for adjustable speed drives (ASDs), uninterruptible power supplies (UPS), and other industrial applications [1]. This configuration features low cost and reliable operation due to the use of a diode rectifier, but it generates highly distorted input line currents and does not have regenerative or dynamic braking capability. These problems can be mitigated by using a back-to- back two-level voltage source converter (B2B 2L-VSC), shown in Fig. 1, where a pulse width modulation (PWM) voltage source rectifier is used to replace the diode rectifier [2].

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The B2B 2L-VSC requires a relatively high number (12) of active switches such as insulated gate bipolar transistors (IG- BTs). It also needs a dc-link capacitor that is responsible for a limited lifespan and increased cost. To reduce the device count and minimize/eliminate the dc-capacitor filter, various converter topologies have been proposed in the literature. The first approach reported in [3]–[5] puts two dc capacitors in cascade and takes their midpoint as one of the input–output terminals, whereby an entire phase leg for the rectifier and/or inverter can be saved. It is also possible to reduce the total number of switches, as the second approach suggests [6], [7], by sharing one of the three phase legs between the rectifier and inverter with proper control. In addition, combined use of dc midpoint connection and phase leg sharing has been proposed in [8], where only four legs are needed to perform three-phase ac to ac con- version with bidirectional power flow and power factor control. Although all the earlier references achieve the goal of reducing the number of switches and thus reducing the

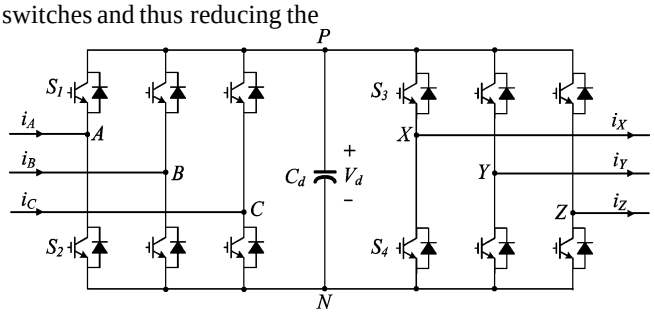


Fig. 1. B2B 2L-VSC.

cost, they unexceptionally have limits or involve complex control due to their un- balanced topological structure. For unidirectional applications, diodes can be used in place of active switches in the rectifier part, such as the VIENNA rectifier [9], three-phase three-switch buck-type rectifier [10], and three-phase three-switch two-level rectifier [11]. These converters may also be regarded as topologies with a saved number of switches, despite their employment of a large number of diodes.

Unlike VSCs that inevitably require the dc-link stage, the matrix converter [12] presents a radical change in topology and directly converts a fixed ac input voltage to an adjustable ac output voltage. It features sinusoidal input–output, controllable power factor, and is capable of bidirectional energy transfer from the supply to the load or vice versa. Since there is no dc- link circuit, the dc capacitor in the VSC is not necessary here, leading to cost reduction as well as improved reliability and longevity.

However, the conventional matrix converter (CMC) normally requires 18 active switches and its switching scheme is complex. The high semiconductor cost and complex control have made this topology less attractive.

Similar to the situation of VSCs, efforts to reduce the number of active switches for a matrix converter have been

made in recent publications [13], [14], where a couple of topological variants such as the sparse matrix converter (SMC) were proposed. The SMC provides equivalent functionality to the CMC. It employs 15 switches with the semiconductor cost still higher than that of the B2B 2 L-VSC. In this paper, a novel one-stage three-phase ac/ac converter topology is proposed. Different from all other existing topologies, this converter has only three legs with only nine active switches for bidirectional ac/ac power conversion

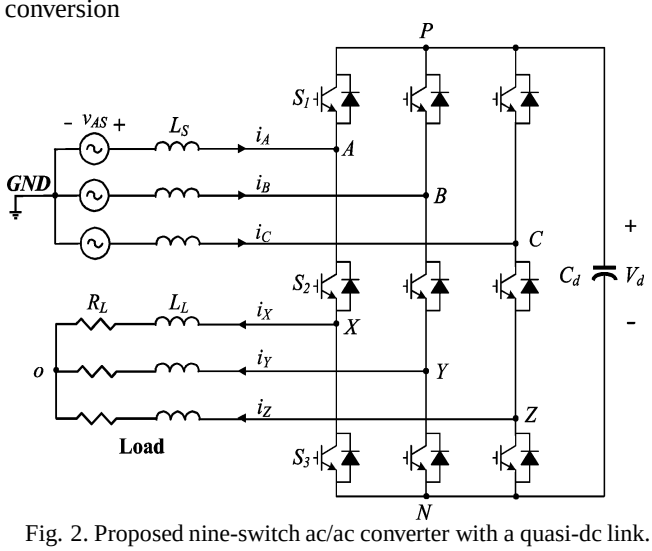


Fig. 2. Proposed nine-switch ac/ac converter with a quasi-dc link.

II. NINE-SWITCH CONVERTER TOPOLOGY

Fig.2 shows the proposed three-phase nine-switch converter topology. This converter has only three legs with three switches installed on each of them. The novelty herein is that the middle switch in each individual leg is shared by both the rectifier and the inverter, thereby reducing the switch count by 33% and 50% in comparison to the B2B 2L-VSC and CMC, respectively. The input power is delivered to the output partially through the middle three switches and partially through a quasi-dc-link circuit.

For the convenience of discussion, we can consider that the rectifier of the nine-switch converter is composed of the top three and middle three switches, whereas the inverter consists of the middle three and bottom three switches.

The converter has two modes of operation: 1) constant frequency (CF) mode, where the output frequency of the inverter is constant and also the same as that of the utility supply, while the inverter output voltage is adjustable; and 2) VF mode, where both magnitude and frequency of the inverter output voltage are adjustable. The CF-mode operation is particularly suitable for applications in UPS, whereas the VF mode can be applied to variable-speed drives.

III. MODULATION SCHEMES

A. Switching Constraint

The reduction of the number of switches in the proposed converter topology imposes certain switching constraints for the switching pattern design. In the B2B 2L-VSC shown in Fig.1, the rectifier leg voltage v_{AN} , which is the voltage at node A with respect to the negative dc bus N , can be controlled by switches S_1 and S_2 in the rectifier, whereas the inverter leg voltage v_{XN} can be controlled by S_3 and S_4 in the inverter. This means that the rectifier and inverter leg voltages can be controlled independently.

TABLE I SWITCHING STATES AND CONVERTER LEGVOLTAGES

(a) Back-to-back converter						
Switching State	S_1	S_2	S_3	S_4	v_{AN}	v_{XN}
1	On	Off	On	Off	V_d	V_d
2	Off	On	Off	On	0	0
3	On	Off	Off	On	V_d	0
4	Off	On	On	Off	0	V_d

(b) Proposed nine-switch converter					
Switching State	S_1	S_2	S_3	v_{AN}	v_{XN}
1	On	On	Off	V_d	V_d
2	Off	On	On	0	0
3	On	Off	On	V_d	0

The B2B 2L-VSC has four switching states per phase, as defined in Table I.

For the nine-switch topology, the control of the input and out- put voltages has to be accomplished through the three switches on each leg. Because the middle switches are shared by the rectifier and inverter, the proposed converter has only three switching states per phase, as listed in Table I. It can be ob- served that switching state 4 for the B2B 2L-VSC does not exist in the nine-switch converter, which implies that the inverter leg voltage v_{XN} cannot be higher than the rectifier leg voltage v_{AN} at any instant. This is, in fact, the main constraint for the switching scheme design of the nine-switch converter.

Carrier-based continuous PWM schemes for modulating the 2L-VSC, such as sinusoidal PWM (SPWM), space vector PWM (SVPWM), and third-harmonic injection PWM (THIPWM), are well established in the literature [15]. The principles of these methods can all be applied to the nine-switch converter but a little modification would be necessary, because when designing the switching pattern for the nine-switch converter, the switching constraint discussed earlier must be satisfied.

Fig.3 illustrates the generalized carrier-based modulation scheme in a single switching period for the nine-switch con-

verter. The rectifier modulating wave v_{mr} and the inverter mod-ulating wave v_{m_i} are arranged such that v_{mr} is not lower than $v_{m\ i}$ at any instant of time. These two modulating waveforms are compared with a common triangular carrier v_c . The generated rectifier and inverter leg voltages v_{AN} and v_{XN} are also shown in the figure. This arrangement guarantees that switch state 4 in the B2B 2L-VSC is eliminated here for the nine-switch converter.

B. Modulation Scheme for CF-Mode Operation

Taking SPWM as an example, Fig. 4 illustrates the mod- ified scheme for CF-mode operation, where m_r and m_i are the rectifier and inverter modulation indexes (defined as

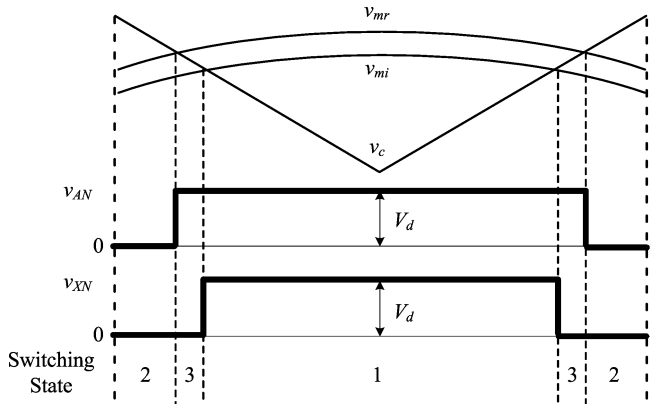


Fig. 3. PWM waveform generation, where switching state 4 of the B2B 2L-VSC is eliminated.

the peak-to-peak magnitude of the sinusoid divided by the peak-to-peak magnitude of the carrier), respectively. The difference between this scheme and the traditional SPWM for 2L-VSC is that here the modulating waves of the rectifier (solid line) and the inverter (dashed line) are placed in a single dc
plane and compared to a common triangular carrier wave. The gate signals are generated at the waveforms' intersections with the carrier. To prevent the modulating waves from intersecting

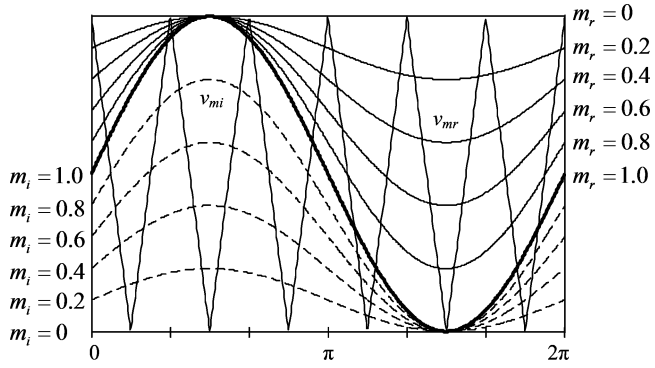


Fig. 4 SPWM scheme for CF-mode operation.

each other, the rectifier's modulating waves are lifted to the top of the dc plane whereas the inverter's are pushed to the bottom by adding proper dc offsets. In this way, the switching constraint of the nine-switch converter can be satisfied. In practice, the rectifier side modulation can be synchronized to the grid via a phase-locked loop (PLL). The freedoms of choosing its modulation index m_r and firing angle α between the modulating wave and the grid can be employed to control the dc voltage and the input power factor. The inverter-side modulation index m_i can be freely selected to adjust the output magnitude. If the inverter's modulating wave is set in phase with the rectifier's, as in the case shown in Fig. 4, both the rectifier and inverter's modulation indexes can simultaneously reach a maximum of unity.

C. Modulation Scheme for VF-Mode Operation

Fig. 5 shows the SPWM modulation scheme for the VF mode of operation. In this case, the inverter's modulation index and phase angle can both be adjusted independently from the rectifier's. In order to satisfy the switching constraint discussed earlier, the sum of the two modulation indexes m_r and m_i of the rectifier and inverter must not exceed 1. For matching the input and output ratings, we limit both of their maximums to 0.5. It can be observed from the figure that both the rectifier and inverter's modulating waves can only be adjusted within half of the carrier's magnitude (which represents the dc volt- age); therefore, the dc voltage v_d of the converter is twice as high as the rated dc voltage of a B2B 2L-VSC with the same ac ratings. This is different from the situation of the CF mode with

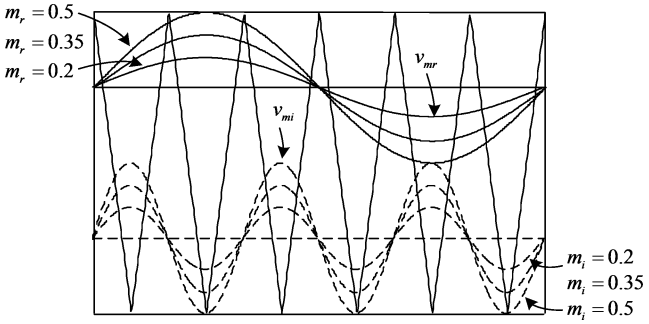


Fig. 5. SPWM scheme for VF-mode operation.

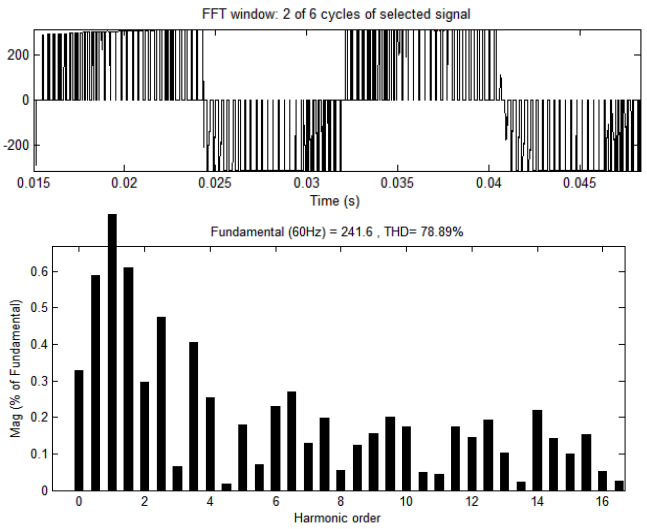
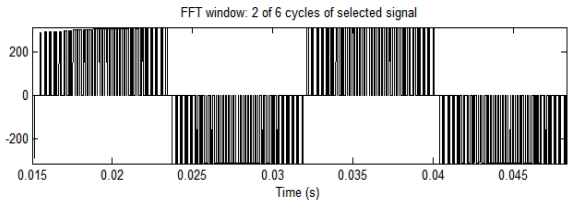


Fig. 6. Rectifier input voltage waveform, spectrum, and THD (CF-mode oper- ation). (a) Rectifier input voltage waveform and spectrum.

Identical input and output phases, in which the dc voltage of the converter can be tightly controlled and maintained at around its rated value. It should be pointed out that although the added dc offsets guarantee that the instant value of v_{mr} is always higher than that of vm i , they are of zero sequence in the three phases and have no effect on the input/output ac magnitudes. In fact, if the inverter's modulation index is selected to be higher than the rectifier's, e.g., mi = 0.5 and mr = 0.2, the fundamental component of the inverter output voltage vXY will be higher than that of the rectifier input voltage vAB .



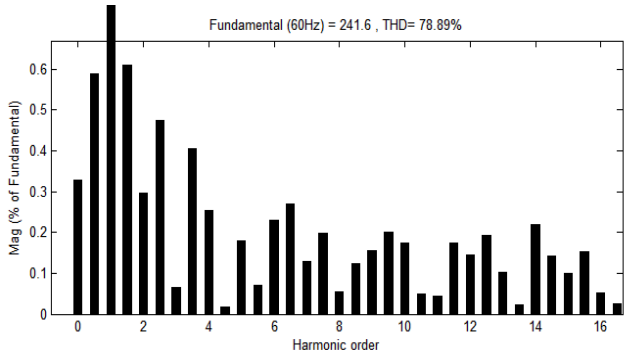
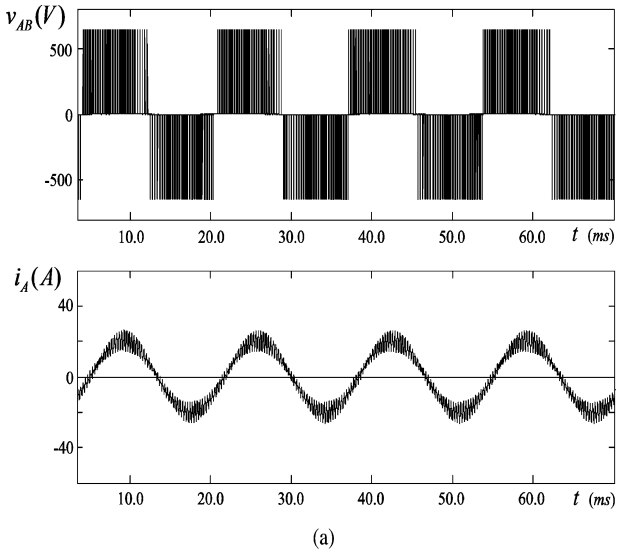
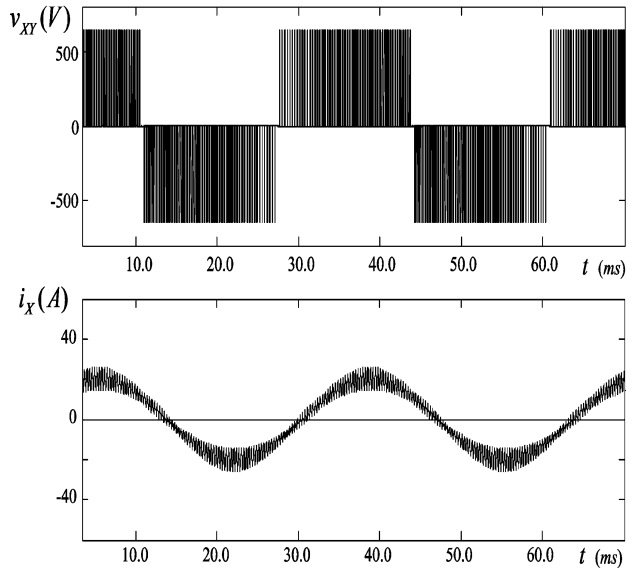


Fig. 7. Inverter output voltage waveform, spectrum, and THD (CF-mode oper- ation). (a) Inverter output voltage waveform and spectrum. (b) THD comparison.



(a)



(b)

Fig. 8. Simulated waveforms of the rectifier and inverter (VF-mode operation). (a) Rectifier input waveforms at 60 Hz. (b) Inverter output waveforms at 30 Hz.

IV. PRINCIPLES OF SVPWM

SVPWM is based on the fact that there are only two independent variables in a three-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase voltage vector may be represented as

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (1)$$

In the SVPWM scheme, the three phase output voltage is represented by a reference vector, which, rotates at an angular speed of $=2\ f$. The task of SVM is to use the combinations of switching states to approximate the locus of V_{ref}, the eight possible switching states of the inverter are represented as two null vector vectors and six active vectors as listed in the Table 2.

TABLE 2: SWITCHING STATES OF THE TWO LEVEL INVERTER

Space vector	Switching State	'On' Switches
Zero Vector	V_7	1,3,5
	V_0	4,6,2
Active vector	V_1	4,6,5
	V_2	4,3,2
	V_3	4,3,5
	V_4	1,6,2
	V_5	1,6,5
	V_6	1,3,2

These vectors (V_1~V_6) can be used to frame the vector plane, which is illustrated in Fig: 9. The rotating reference vector can be approximated in each switching cycle by switching between the adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such a way that only one leg is affected in every step. For a given magnitude and position V_{ref}, can be synthesized by three nearby stationary vectors, based on which, the switching states of the inverter can be selected and gate signals for the active switches can be generated. When V_{ref}, passes through sectors one by one, different sets of switches will be turned on and off .

As a result, when V_{ref}, rotates one revolution in space, the inverter output voltage varies, one cycle over time. Three stationary vectors can synthesize the reference V_{ref}. The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period Ts of the modulation scheme. The dwell time calculation is based on 'volt-second balancing' principle, that is, the product of the reference voltage V_{ref} and sampling period Ts equals the sum of the voltage multiplied by the time interval of chosen space vectors.

For example, when V_{ref} falls into sector I as shown in Fig: 10, it can be synthesized by V_1, V_2 and V_0.The volt second balance equation is

$$V_{ref}T_s = V_1T_0 + V_2T_b + V_0T_0$$
$$T_S = T_a + T_b + T_c \quad (2)$$

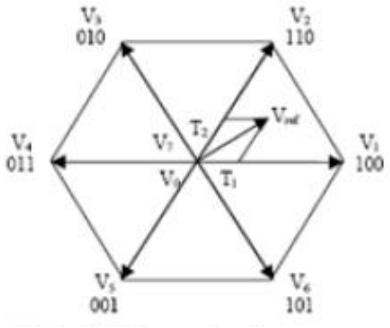


Fig.9. Switching vectors hexagon

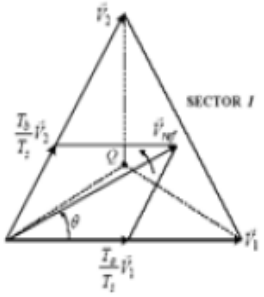


Fig.10. V_{ref} synthesized by V_1, V_2 and V_0

For linear modulation range, the dwell times can be calculated as:

$$T_a = \frac{\sqrt{3}T_s V_{ref}}{V_d}\sin\left(\frac{\pi}{3}-\theta\right)$$
$$T_b = \frac{\sqrt{3}T_s V_{ref}}{V_d}\sin(\theta), 0 \le \theta \le \frac{\pi}{3} \quad (3)$$
$$T_0 = T_s - T_a - T_b$$

5. SEGMENT SPACE VECTRO MODULATION

The sector judgment and application time of active vector for all SVM strategies are the same. The choice of the null vector determines the SVM scheme. There are a few options: the null vector V_0 only, the null vector V_7 only, or a combination of the null vectors. A popular SVM technique is to alternate the null vector in each cycle and to reverse the sequence after each null vector. This will be referred to as the symmetric 7-segment technique. Fig. 11 shows conventional 7-segment switching sequences of sector I. It is shown that the sequence V_0-V_1-V_2-V_0 is used in the first $T_s/2$, and the sequence V_0-V_2-V_2-V_0 is used in the second $T_s/2$. The sequences are symmetrical. The switching frequency is the same as sampling frequency of the inverter.

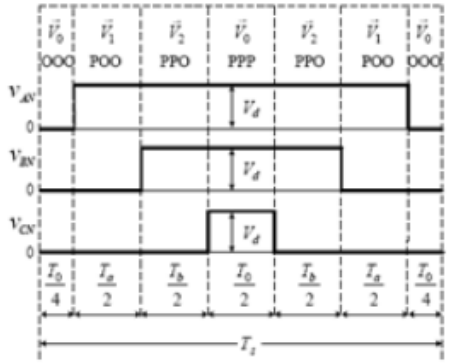
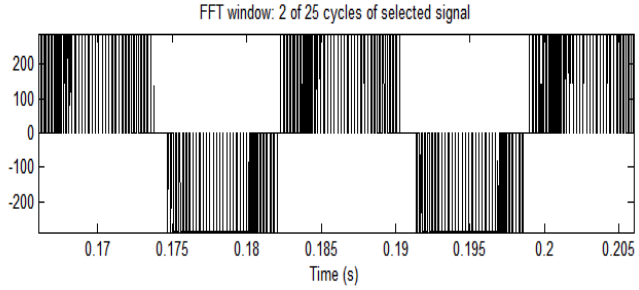


Fig.11. 7-Segment Switching Sequence for V_{ref} in sector I



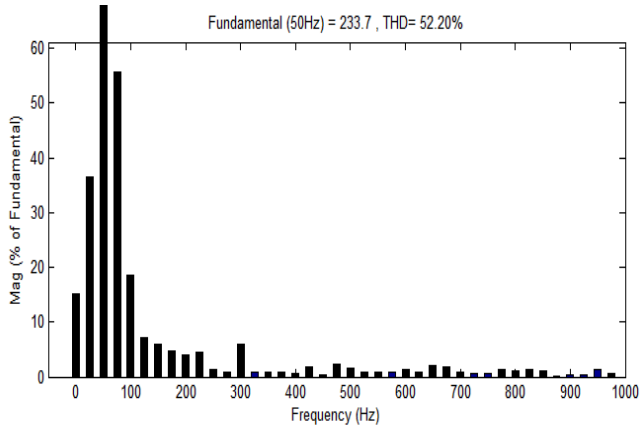


Fig. 12. Rectifier input voltage waveform, spectrum, and THD (CF-mode oper- ation). (a) Rectifier input voltage waveform and spectrum.

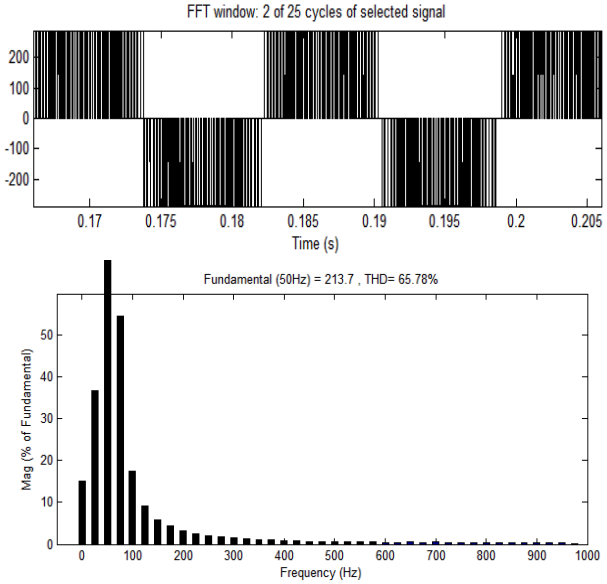


Fig.13. Inverter output voltage waveform, spectrum, and THD (CF-mode oper- ation). (a) Inverter output voltage waveform and spectrum. (b) THD comparison.

IV. SIMULATION ANALYSIS

The performance of the proposed nine-switch converter topology is simulated with the Matlab/Simulink software. In the simulation, the utility supply is rated at 208 V and 60 Hz with a source inductance of Ls = 2.5 mH. The converter is rated at5 kVA and is driving a three-phase RL load of RL = 8 Ω and LL= 2.5 mH. The dc capacitor Cd is 2350 µF. SVPWM method is used to modulate the converter for its superior performance over SPWM and higher dc voltage utilization. The rectifier is controlled by a vector control scheme with unity power factor operation. The inverter output voltage is not detected, and there- fore, is not tightly controlled. The switching frequency of both rectifier and inverter is 3240 Hz. Both CF and VF modes of operation are investigated.

A. CF-Mode Operation

Fig. 6(a) shows the simulated waveform of the rectifier input voltage v_{AB} and its harmonic spectrum with the converter operating in the CF mode. The modulation indexes for the rectifier m_r and inverter m_i are both set at 0.9 and the dc voltage is maintained at 320 V. The frequency of

the dominant switching harmonics is centered around 3240 Hz, which is the carrier frequency and also the switching frequency of the converter. The low-order harmonics are negligibly small.

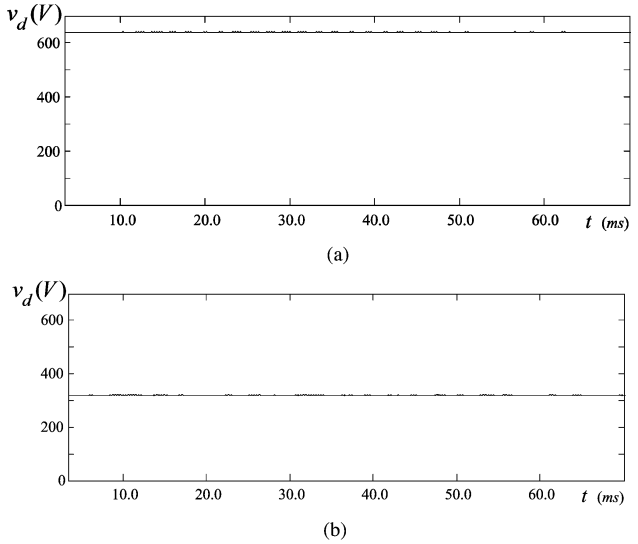


Fig. 9 Comparison of dc voltage and inverter output THD with full utility supply (VF-mode operation). (a) DC voltage of nine-switch converter. (b) DC voltage of B2B 2L-VSC.

Fig. 7(a) shows the simulated waveform and spectrum of the inverter output voltage v_{XY} with a fundamental frequency of 60 Hz. It is interesting to note that the inverter output voltage waveform, its fundamental component, and THD are very close to those of the rectifier given in Fig. 6.

Fig. 7(b) gives the THD comparison of the inverter output voltage v_{XY} between the nine-switch converter and the B2B 2L-VSC, with respect to the inverter modulation index m_i. It can be seen that the inverter out- put THD characteristics are identical to that of the rectifier input.

B. VF-Mode Operation

Fig. 8 shows the simulated rectifier input and inverter output waveforms when the converter operates in the VF mode. The rectifier operates at 60 Hz while the inverter operates at 30 Hz. The modulation indexes for the rectifier and inverter are both 0.45. The figure illustrates that the rectifier and the inverter can operate independently with different fundamental frequencies.

Fig. 9(a) and (b) presents the VF-mode dc voltage comparison between the nine-switch converter and the B2B 2L-VSC. Due to the boost nature of the rectifier, the dc voltage vd of the nine-switch converter in VF mode becomes twice that in the CF mode, which is also the rated value of a B2B 2L-VSC with identical ac ratings. A THD comparison of the inverter output voltage vXY versus the normalized inverter modulation index mi /mi, max is shown in Fig. 9(c), where the maximum modulation index mi, max for the nine-device converter and the B2B 2L-VSC are 0.5 and 1, respectively. It can be noted that with the same ac-side voltage magnitudes, the THD of the nine- switch converter output is much higher than that of a competitive B2B 2L-VSC because of the lower modulation index that the nine-switch converter is working at.

VI. CONCLUSION

A nine-switch PWM ac/ac converter topology was proposed in this paper. The topology uses only nine IGBT devices for ac to ac conversion through a quasi dc-link circuit. Compared with the conventional back-to-back PWM VSC using 12 switches and the matrix converter that uses 18, the number of switches in the proposed converter is reduced by 33% and 50%, respectively. The proposed converter features sinusoidal inputs and outputs, unity input power factor, and low manufacturing cost. The operating principle of the converter was elaborated, and modulation schemes for constant and VF operations were developed. However, the VF-mode version requires IGBT devices with higher ratings and dissipates significantly higher losses, and thus, is not as attractive as its counterpart.

Space vector Modulation Technique has become the most popular and important PWM technique for Three Phase Three leg AC-AC converter for the control of AC Induction, Brushless DC, Switched Reluctance and Permanent Magnet Synchronous Motors. In this paper first comparative analysis of Space Vector PWM with conventional SPWM for a three phase three leg AC-AC converter is carried out. The Simulation study reveals that SVPWM gives 15% enhanced fundamental output with better quality i.e. lesser THD compared to SPWM. PWM strategies viz. SPWM and SVPWM are implemented in MATLAB/SIMULINK software and its performance is compared with conventional PWM techniques. Owing to their fixed carrier frequencies cf in conventional PWM strategies, there are cluster harmonics around the multiples of carrier frequency. PWM strategies viz. Sinusoidal PWM and SVPWM utilize a changing carrier frequency to spread the harmonics continuously to a wideband area so that the peak harmonics are reduced greatly.

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