Transcendental and Optimized Digital Designing using Reversible Logic

Divyansh Mathur, Prachi Singh, Sunita Singh

Abstract – In [1] we have presented a novel design of different Digital Arithmetic and Logic Units using basic Reversible Gates. The current issue presents andemphasises on the use of Ultimate Optimized Design of digital circuits such as Adders, Subtracters, and 1-Bit Comparator. Furthermore, the Optimized Design does not give any ambiguous values in the terms of Quantum Cost associated with the circuit.

Index Terms –Ancillary Inputs, Quantum Cost, TR Gate.

I. INTRODUCTION

The approach in the Reversible Logic Design differs significantly from the traditional Combinational Logic Design. In Reversible Logic Circuit, the number of input lines should be equal to the number of output lines with each output line being used only once thereby making the resulting circuit acyclic[10]. Thus a Reversible Logic Gate is an n-input, n-output device with one-to-one mapping. This helps in the determination of the outputs from the inputs and vice-versa, i.e. there is one-to-one correspondence between the input and the output vectors. The main challenges are reducing the hardware complexity, delay, quantum cost, power dissipation, garbage outputs and the overall number of constant ancillary inputs used in the Logical Unit's Design.

Energy loss in Digital Designing is an important factor for marking the level of performance. While some portion of the energy is dissipated due to non-ideality of switches, the other results from the quality of materials used. Though heat loss has been dramatically reduced by complex integration levels and high-end fabrication processes, the part of reducing energy dissipation in Digital Circuits is still left undone. It is here that the Reversible Logic shows its effect and its applications in promising computer paradigms with applications in emerging technologies such as Quantum Computation, Quantum Dot Cellular Automata, Optical Computing etc.[4, 5, 6, 7, 8, 9]. Bennet[11] had observed that if a computation is carried out on Reversible Logic, zero energy dissipation is possible, as the amount of energy dissipated in a system is directly in relation to the number of bits erased during that computation.

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Since Normal Combinational Logic Circuits dissipate heat for every bit of information lost during their operation, the recovery of a piece of information once lost is completely impossible. However, if the same circuit is constructed using the Reversible Logic Gates, chances are high not only of therecovery of that piece of information but also reducing the heat losses. Demonstrated by R. Landauer in 1960s, the energy dissipation for every bit of information exchange, associated with even high-tech systems designed with traditional and irreversible logic was numerically equal to kT.ln2; wherein k is described as the Boltzmann Constant and T as the absolute temperature at which the operation is being performed[1].

As stated previously, designing of digital circuits using the Reversible Logicis an on a grow technique which is steadfastly paving its way into Digital Electronics, Quantum Cost is one of the major factors playing a pivotal role in the designing of Arithmetic and Logical Units.

Quantum Cost, the cost of a circuit, refers to the overall expenses,pertaining to the use of Reversible Logic Gates for synthesising a given Logical Function, incurred in designing of the circuit in terms of the cost of the primitive Reversible Logic Gates used. The Quantum Cost of the circuit is determined by calculating the *already known* cost of the primitive gates required for realizing the Arithmetic and Logic Circuit Units.

Other factors effecting the realization of different Digital Arithmetic and Logic Circuits are *Ancillary Inputs,Garbage Outputs*, and *Delay*. *Ancillary Inputs* are the inputs which have a constant value of either 0 or 1, provided at the input terminals of the Reversible Logic Gates, and have to be maintained at a constant value in order to synthesise the given Logical Function, as per the requirements.On the other hand *Garbage Outputs* are those output vectors that are left unutilised. Though the *Garbage Outputs*do not perform any useful operation, yet they are present in order to maintain the reversibility of the circuit[1].

As the Moore's Law holds and will alwayscontinue to hold, the number of chip components keep getting doubled in every one and a half years;the designing of digital circuits using the traditional combinational logic would not only cause a high rate of dissipation of energy in form of heat and information loss in the circuits, but also reduce the circuit's performance and life to a great extent. Designingin this way would not fulfil the desired purpose of achieving the efficiency, the demand in today's silicon world.

This paperis thereforepresented here to meet the much required standards for the need of efficientandoptimizeddesign models of digital circuits such as Adders, Subtracters, and 1-Bit Comparatorusing onlybasic Reversible Logic Gates who's Quantum Cost is known, established, and unambiguous.

II. BASIC REVERSIBLE GATES

A. *BVF Gate*

With Quantum Cost of two, the BVF Gate is a 4x4 Reversible Gate described as follows:

I_V = (A, B, C, D)

O_V = (P=A, Q=A⊕B, R=C, S=C⊕D)

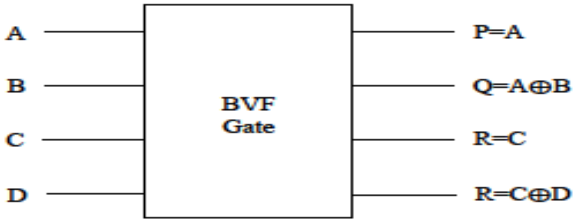

Figure 1: BVF Gate

B. *Feynman/CNOT Gate[15]*

It's a 2x2 Reversible Gate having a Quantum Cost of one and described as under:

I_V= (A, B)

O_V = (P=A, Q=A⊕B)

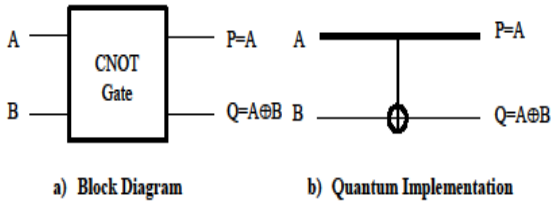

Figure 2: Feynman/CNOT Gate

C. *Fredkin Gate[13]*

The Fredkin is an advanced 3x3 Reversible Gate with a Quantum Cost of five and description given by:

I_V = (A, B, C)

O_V = (P=A, Q=$\bar{A}$B+AC, R=AB+$\bar{A}$C)

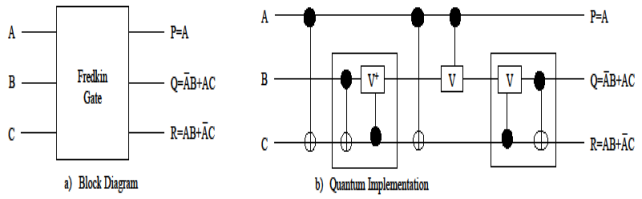

Figure 3: Fredkin Gate

D. *Peres Gate[14]*

It's a 3x3 Reversible Gate, constructed from one CNOT and one Toffoli Gate having a Quantum Cost of four and described by:

I_V = (A, B, C)

O_V = (P=A, Q=A⊕B, R=(AB)⊕C)

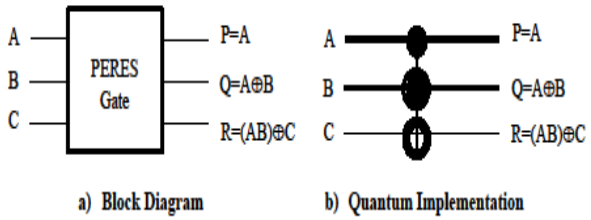

Figure 4: Peres/New Toffoli Gate

E. *Toffoli Gate[12]*

It has a Quantum Cost of five and described by:

I_V = (A, B, C)

O_V = (P=A, Q=B, R=(AB)⊕C)

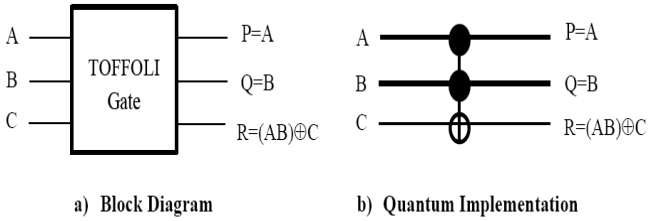

Figure 5: Toffoli Gate

III. DESIGN MODELS USING REVERSIBLE GATES

A. *Design Model of Half Adder*

A Half Adder is a Logical CircuitUnit designed to add two binary bits and provide the output in terms of Sum and Carry.

SUM = A⊕B

CARRY = AB

The truth table is illustrated as:

Table 1: Half Adder Truth Table

INPUTS		OUTPUTS	
A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The Design Logic stated in [1] was given by:

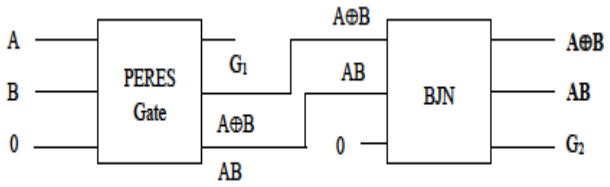

Figure 6: Half Adder using Peres and BJN Gate

The *optimized* design of the circuit is now shown:

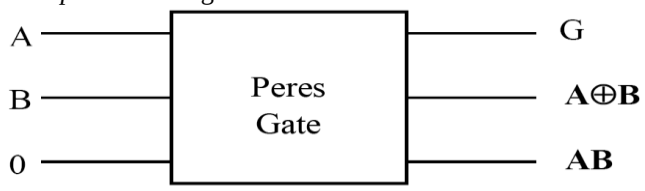

Figure 7: Optimized Half Adder

With this *optimized* design approach we can hereby conclude that this design is *complete in itself* and requires *no additional*

modifications when Quantum Cost and other parameters are concerned. The following table establishes the facts stated above:

Table 2: Comparison of Different Designs of Half Adder

PARAMETERS	*Figure 6*	*Figure 7*
Garbage Outputs	2	1
Logic Gates Used	2	1
Constant Ancillary Inputs Number	2	1
Quantum Cost	9	4
Improvement in Quantum Cost	+55.56%	

B. *Design Model of Half Subtracter*

Made for the purpose of carrying out the task of finding the difference between twobinary bits, the Logical Unit of the Half Subtracter is discussed here. The two output terms are as follows:

DIFFERENCE = A⊕B

BORROW = $\bar{A}$B

Table 3: Half Subtracter Truth Table

INPUTS		OUTPUTS	
A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

The conventional logic in [1] was:

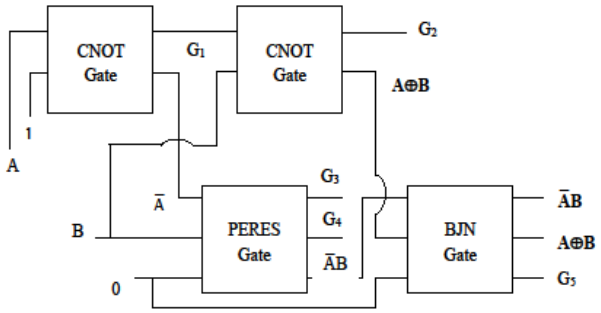

Figure 8: Half Subtracter Using CNOT, PERES and BJN Gates

Now the*optimized* design for the same is:

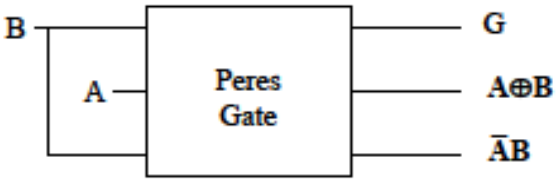

Figure 9: Optimized Half Subtracter

From the above two figures we can conclude that the *optimized* design is not only *simple in construction* but also *efficient* in terms of the *Quantum Cost*.

Table 4: Comparison of Different Designs of Half Subtracter

PARAMETERS	*Figure 8*	*Figure 9*
Garbage Outputs	5	1
Logic Gates Used	4	1
Constant Ancillary Inputs Number	2	0
Quantum Cost	11	4
Improvement in Quantum Cost	+63.64%	

C. *Design Model of Full Adder*

An advancement of the Half Adder, the Full Adder is a circuit designed to perform the summation operation onthree binary bits.

The method cum operation of the Logical Unit is same as that of the Half Adder but with an additional binary bit.

The outputs of the Full Adder are also represented as SUM and CARRY, and these are described by the following values:

SUM = A⊕B⊕C

CARRY = {(A⊕B)C}+(AB)

The value of variable CARRY can also be given by {(A⊕B)C}⊕(AB), as they yield same results.

Thetruth table of the Full Adder is given in the table below:

Table 5: Truth Table of Full Adder

INPUTS			OUTPUTS	
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Keeping in mind the values of the outputs, the Half Adder has been described and realizedusing two cascaded Peres Gates with a *minimum* Quantum Cost of 8. It has been shown in [17] and [19] that any R*eversible Logic* realisation of *Full Adder* Circuit includes *at least two garbage outputs* and *one constant input*. The authors in [16-19] have given a Quantum Cost efficient Reversible Full Adder Circuit that is realised using two 3x3 Peres Gates only.

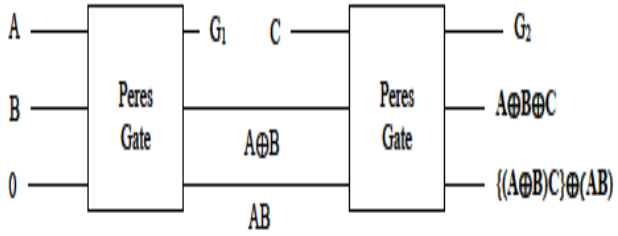

Figure 10: Full Adder Using Peres Gate

The optimized design for the same follows as:

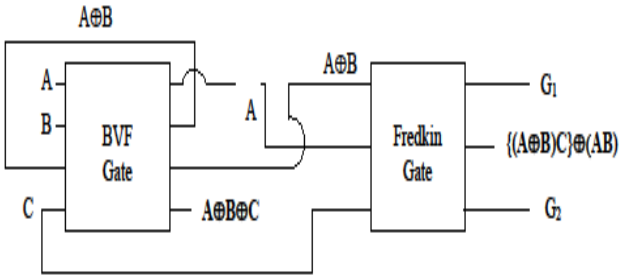

Figure 11: Optimized Full Adder

In this circuit not only has the *Quantum Cost* been *reduced* but the *Constant Ancillary Input removed*, implying that the above stated design and its corresponding references can follow this new improved model. Here the energy dissipation is considerably lowered as there is no constant ancillary input which may consume power from any external source.

Further we would like to add that we don't disagree on the proposed designs but simply present our new *optimized* model which can be used to improve circuit performance and life.

The Comparison Table illustrates the things that were stated above:

Table 6: Comparison of Different Designs of Full Adder

PARAMETERS	*Figure 10*	*Figure 11*
Garbage Outputs	2	2
Logic Gates Used	2	2
Constant Ancillary Inputs Number	1	0
Quantum Cost	8	7
Improvement in Quantum Cost	+12.5%	

D. Design Model of Full Subtracter

With similar working as that of its counterpart, the Full Subtracter is used to subtract three and not just two binary bits. The output values are:

DIFFERENCE = A⊕B⊕C

BORROW = {(A⊕B)'C}⊕(ĀB)

Truth Table is shown below:

Table 7: Truth Table of Full Subtracter

INPUTS			OUTPUTS	
A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The design shown below is taken from [2] & [3].

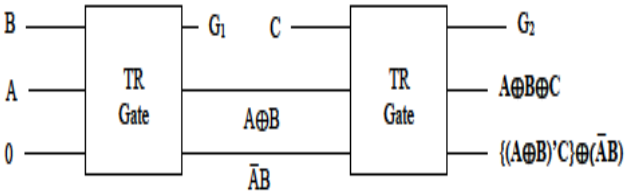

Figure 12: Full Subtracter Using TR Gate

The designing of Subtracters has always been an issue in terms of Quantum Cost. Instead of using a *proposed gate exclusively for subtracters*[2], we are citing an *optimized* model which doesn't give any *ambiguous* values in terms of Quantum Cost, and uses *basic Reversible Gates* in place of the *proposed TR Gate*. Although the *optimized model* isn't efficient in terms of number of gates used & the number of garbage outputs, but still we have tried our level best in maintaining the Quantum Cost of the circuit taking into account the *upper*as well as the *lower bound limit* of the *proposed TR Gate's Quantum Cost*. If the *upper bound* is taken as 6[2] then overall cost jumps to 12 while the lower bound of 4[3] drops its value to 8.

With this in mind, the *optimized* circuit undoubtedly matches the *minimum* value of Quantum Cost.

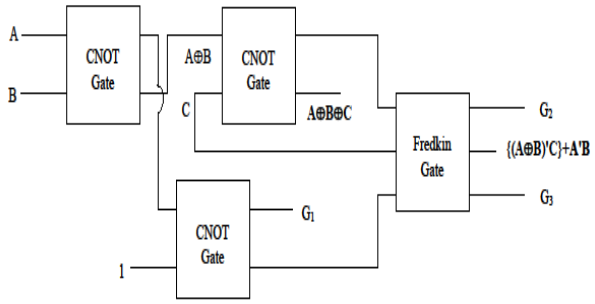

Figure 13: Optimized Full Subtracter

The analytical study is shown in the table below:

Table 8: Comparison of Different Designs of 1-Bit Comparator

PARAMETERS	*Figure 12*		*Figure 13*
Garbage Outputs	2		3
Logic Gates Used	2		4
Constant Ancillary Inputs Number	1		1
Quantum Cost	12 (if taken 6)	8 (if taken 4)	8
Improvement in Quantum Cost	+33.33% (for 12) & ±0% (for 8)		

E. Design Model of 1-Bit Comparator

A 1-Bit Comparator is a Logical Circuit designed to compare two binary numbers, each having one bit. The output is taken in three states, $F_{A<B}$, $F_{A=B}$ and $F_{A>B}$, respectively.

By the name it has, the 1-Bit Comparator logic circuit works by comparing each of the bits of the two binary input numbers. When one bit is at logic low and the other at logic high, comparison is done by checking which bit belongs to which number and the output can either be $F_{A<B}$ or $F_{A>B}$. On the other hand, when both the bits are at logic low or logic high, then the output is certainly $F_{A=B}$.

The corresponding truth table is shown:

Table 9: 1-Bit Comparator Truth Table

INPUTS		OUTPUTS		
A	B	$F_{A<B}$	$F_{A=B}$	$F_{A>B}$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Based on the above truth table the output assumes form in three different cases elaborated as:

$F_{A<B} = \bar{A}B$

$F_{A=B} = \bar{A}\bar{B}+AB = (A \oplus B)'$

$F_{A>B} = A\bar{B}$

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The design published in [1] is as follows:

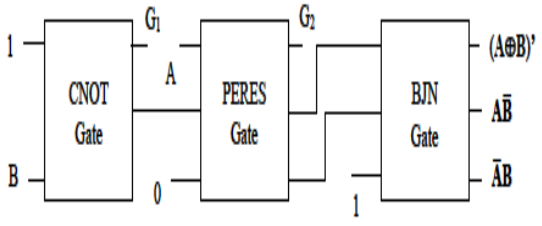

Figure 14: 1-Bit Comparator using CNOT, Peres and BJN Gate

The *optimized* design can be illustrated by:

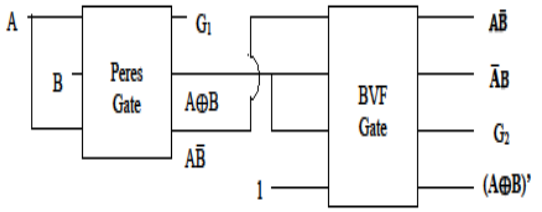

Figure 15: Optimized 1-Bit Comparator

It can now be inferred from the above two figures, Figure 14 and Figure 15 respectively, that the design as well as the circuit complexity, the Quantum Cost, are reduced extensively; thus making the *optimized* model efficient in overall terms.

Thedifferences are now clearly tabulated below:

Table 10: Comparison of Different Designs of 1-Bit Comparator

PARAMETERS	*Figure 14*	*Figure 15*
Garbage Outputs	2	2
Logic Gates Used	3	2
Constant Ancillary Inputs Number	3	1
Quantum Cost	10	6
Improvement in Quantum Cost	+40%	

IV. CONCLUSION

It's now clear from the above design methodologies how Reversible Logic has redefined the way and the approach in which the Logical and Arithmetic Units were taken into consideration and designed using the conventional combinational logic techniques.

The paper has precisely brought into light the much *hyped and unexplored world* of Reversible Logic in the area of Digital Electronics.

The *optimized* models and the comparative analytical tables which employed the techniques of Reversible Logic have shown how the proposed designs have made the basic logical units economical and justifiable.

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