A Review of Memory Circuit Design Trend in Nanotechnology

Yogesh N. Thakre, Shubhada S. Thakare, Devendra S. Chaudhari

Abstract**—*****DRAM is type of volatile memory. Nowadays semiconductor memory is capable to store large data in small area. In past SRAM is more preferable as compared to DRAM because of its high speed operation, large noise margin and logic compatibility. However, due to its large cell area and high power consumption, SRAM has limitations when expanding the array size beyond a certain level in process variation. This paper reviews the history of RAM from SRAM to DRAM. It also suggests the day by day DRAM is more preferable as compare to SRAM because of cell area decreases as number of transistor decreases from SRAM to DRAM design.***

Index Terms— Cell, Cell area, Dynamic RAM (DRAM), Static RAM (SRAM), 3T-1D (Three transistor- one diode), etc.

I. INTRODUCTION

Due to continuous technological changes it is possible to perform same read/ write operation with minimum number of transistor. Hence, with the help of nanotechnology it is possible to continuous transistor density change is possible.[1] Generally a computer uses RAM to temporarily hold instructions and data necessary for the CPU (Central Processing Unit) to process some tasks. In past decade memory occupy 90% of chip area from total embedded chip. So not only area gets increases but also cost. Nowadays current technology demands large storage area in small space. Traditionally, out of total SRAM 6T SRAM is more preferable embedded memory RAM because of its high speed of operation, large noise margin and logic compatibility. However, due to its large cell area and high power consumption it is not suitable for process variation. For this one alternative solution is gain cell memory. Gain memory cell performs as a DRAM cell depending on gated diode capacitance with low power feature and internal voltage gain which improves the operation speed. [2] The DRAM cell consists of a capacitor to store binary information and a transistor to access the capacitor. Cell information is degraded mostly due to a junction leakage current at the storage node because of capacitor. Therefore the cell data must be read and rewritten periodically even when memory arrays are not accessed. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory. The advantage of DRAM is its structural simplicity; only one transistor and a capacitor are required per bit, compared to four or six transistors in SRAM. This allows DRAM to reach very high densities and more applicable embedded memory.

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Yogesh N. Thakre, Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India.

Shubhada S. Thakare, Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India.

Dr. Devendra S. Chaudhari, Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India.

II. MEMORY OVERVIEW

An overview of existing memory devices is shown in Figure 1.1, classified in the way the information is stored. If the information is stored nonvolatile, then the power supply can be turned off and the information remains stored. But, this is not the case for two remaining memory groups. Non-volatile of memory is permanent type of memory. The tree diagram of memory overview is shown below.

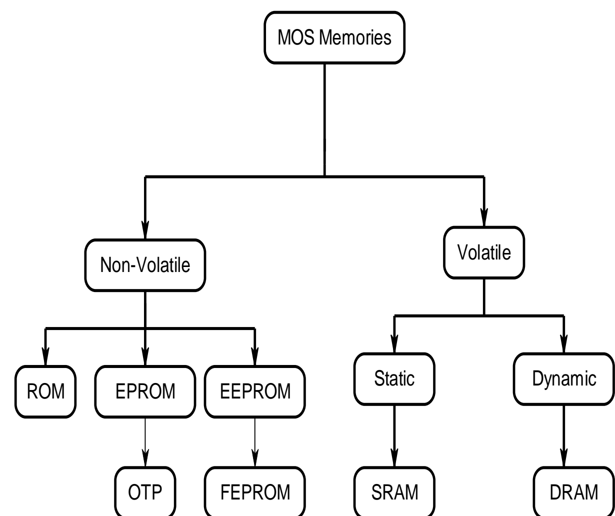

Fig. 1.1 Overview of MOS Memories

The meaning of the individual memory names is summarized in Table I.

TABLE I Commonly Used Memory Names

ROM	Read Only Memory
EPROM	Electrically Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
OTP	One Time Programmable
FEPROM	Flash Erasable Programmable Read Only Memory
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory

III. ARCHITECTURE OF SRAM CELL

A typical SRAM block consists of cell arrays, address decoders, column multiplexers, sense amplifiers, input/output (I/O), and a control unit. In the following, the functionality and design of each component is briefly discussed.

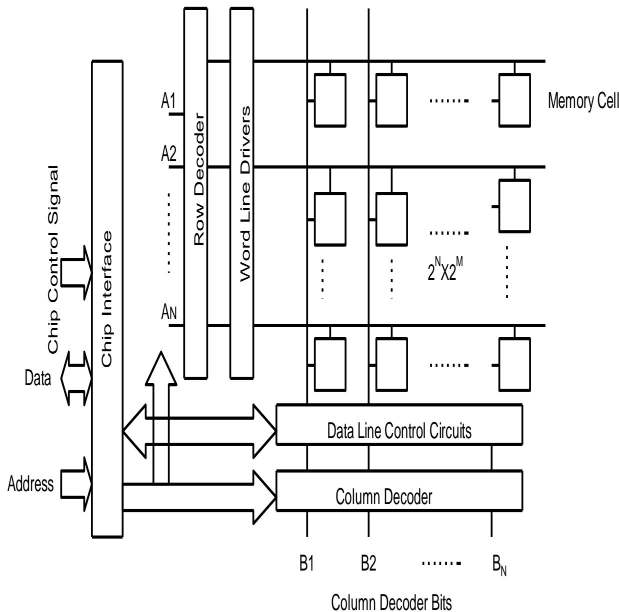

Fig. 1.2 Architecture View of SRAM

A. *Final Stage*

Figure 1.2 shows a SRAM cell. In a SRAM cell, the fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. The cell has a single bit line. True and complementary read and write signals are used in place of a single word line. The pull-down N-MOS transistors and the pass-transistors reside in the read path. The pull-up P-MOS transistors and the pass-transistors, on the other hand, are in the write path. Traditionally, all cells used in an SRAM block are identical (i.e., corresponding transistors have the same width, threshold voltage, and oxide thickness) which results in identical leakage characteristic for all cells. [5]

B. *Cell Array*

The data storage structure or core consists of individual memory cell arranged in array of horizontal rows and vertical columns. Each cell is capable of storing one bit of binary information. The size of the cell array depends on both performance and density requirements. Generally speaking, as technology shrinks, cell arrays are moving from tall to wide structures. In this structure, there are 2^N rows, also called word line, and 2^M columns, also called bit line. Thus the total number of memory cell in this array is 2^N X 2^M. [5]

C. *Address Decoder*

To access particular memory cell i.e. particular data bit in this array, the corresponding word line and bit line must be activated. Although the logical function of an address decoder is very simple, in practice designing it is complicated. To overcome the pitch-matching problem and reduce the effect of wire’s capacitance on the delay of the decoder, the address decoder is often broken into two pieces. The first piece, called pre-decoder, is placed before the long decoder wires and the second part, row decoder, which usually consists of a single NAND gate and buffers for driving the word-line capacitance, is pitch-matched and placed next to each row as shown in Figure.1.2 [5]

D. *Column Multiplexers and Sense Amplifiers*

Column multiplexing is inevitable in most SRAM designs because it reduces the number of rows in the cell array and as a result increases the speed. Since during a read operation one of the bit or bit-line is partially discharged, a sense amplifier is used to sense this voltage difference between bit and bit-bar lines to create a digital voltage. To make the circuit more robust to noise, the sense amplifier is switched when the voltage difference between bit and bit-bar lines becomes 100–200 mV. [5]

E. *Control Unit*

The control unit generates internal signals of the SRAM, including the write and read enable signals, the pre-charge signal, and the sense amplifier enabler. [5]

IV. PROCESS VARIATION ON RAM

In this paper, we have discussed various SRAM and DRAM design. Compare it on the basis of scaling limitations, area required, number of transistor required, etc. The SRAM cell consists of latch so the cell data is kept as long as power is turned on and refresh operation is not required.

A. *Typical 8T SRAM Cell*

The 8T SRAM cell shown in Figure1.3 When read operation is performed read bit line RBL is precharged to VDD. The read operation is going on when RWL is high. RBL either remains at VDD or ground depends on internal node contains 0 or 1 respectively. At write operation write word line WWL is get activated and the corresponding values from the bit line. Here it uses a buffered read to isolate the internal nodes of the cell from read path. [6]

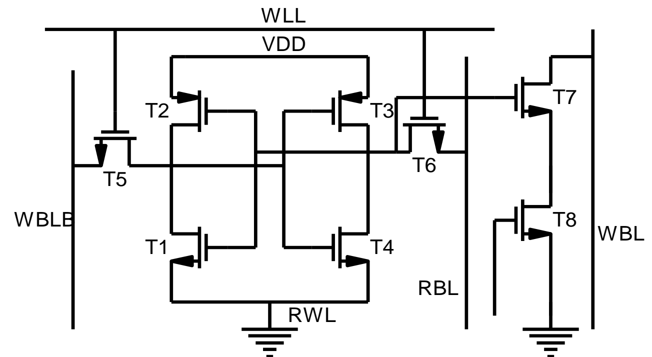

Fig. 1.3 SRAM Cell with 8 Transistors

B. *Six Transistor SRAM Cell*

In six transistors SRAM cell the each bit required four transistors. This storage node has two stable state ‘0’ and ‘1’. Two accesses these cross coupled invertors additional transistor are required. So typically it required six transistors to store one memory bit. When word line (WL) is get activated gives direct access to cell with the help of transistor M5 and M6. There is presence of dual bit line i.e. BL and BLBAR improves noise margin over single bit line. The design of a basic SRAM cell is shown in Figure1.4. [6] In order to read the stored data, one side of the cell typically discharged one of two precharged bitlines. If there is any variation in the gate length or threshold voltages in the cells transistor (*T1 or T2)* can vary the current driving capability of read path. Also, leakage is the main problem in SRAM cell.

There are three strong leakage paths in one 6T SRAM cell since only one transistor is 'off' along each path[6]. Such an SRAM structure consumes considerable amount of static current in order to preserve data in the cell.

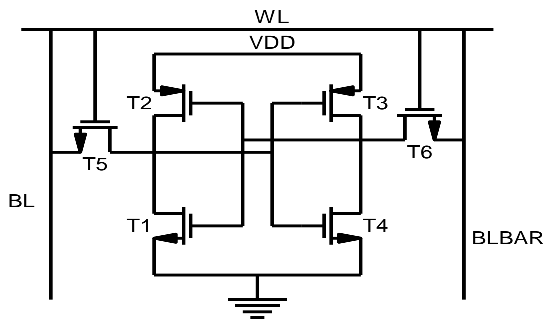

Fig. 1.4 SRAM Cell with 6 Transistors

C. Four Transistor SRAM Cell

In this 4T SRAM cell with the help of four transistor read/write operation is performed. Here 4T SRAM cell using a supply voltage of 0.9V. In this 4T SRAM transistor T3 acts as drive transistor and T1 acts as load transistor. When '1' stored in cell load and driver transistor is ON. ST node pulled to ground by driver transistor T3 and STB node pulled to VDD by load transistor T1. When '0' get stored in cell load and driver transistor are OFF and data retention without refresh cycle satisfying when we use leakage current of access transistor, especially sub threshold current of access transistor.[6]

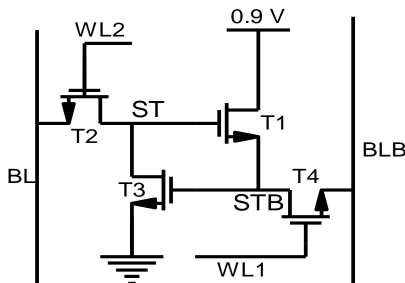

Fig. 1.5 SRAM Cell with 4 Transistors

D. Two Transistor DRAM Cell

The 2T DRAM cell is most popular DRAM cell for on chip application. During a write, WBL is activated along with data & finally when WL (write line) is activated data get stored on store node. In this DRAM cell data is stored by extra device i.e. capacitor. In this cell reading the value from cell is more complex than the writing the data in the cell. During read operation RBL is get activated & when RL get low data get read. When logical '1' is there RBL becomes low while logical '0' will leave the value of RBL unchanged. [2]

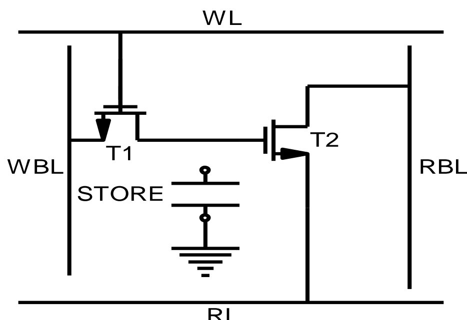

Fig. 1.6 Two Transistor DRAM Cell

This readout phase is allowed to continue for a present margin of time. During this time a logical one drop the voltage on RBL to some level Vr. Vrbl compared with some reference voltage Vref such that Vdd>Vref>Vr. Via a difference sense amplifier. A refresh operation is required, as the read process is destructive. But there is one complication with 2T DRAM cell is that Vrbl line will not drop more than two n-transistor threshold below the Vdd during the read operation. The reason behind this adjustment bit in the same column has a one stored. If the read bit line should drop more than two thresholds then this transistor will on & keep the bit line from falling further, but practically it is more adequate for current sensing amplifier. Sensing the difference between this read bit line and the reference voltage requires a circuit structure called differential sense amplifier. [7]

E. One-Transistor DRAM Cell

The one-transistor DRAM cell has become the industry-standard dynamic RAM cell in high-density DRAM arrays. It has explicit storage capacitor. It means that a separate capacitor must be manufactured for each storage cell, instead of relying on the gate and diffusion capacitances of the transistors for data storage.

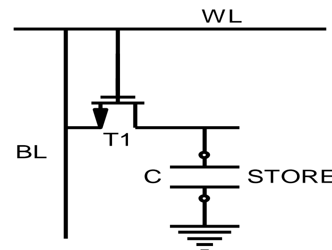

Fig. 1.7 One Transistor DRAM Cell

In the "write" operation, after the word line is enabled, the data are written into the cell through the Ml transistor and stored at the storage capacitor. The read operation is destructive. When the charge stored in the storage cell is shared with the bit line, its charge can he changed significantly (destructed).

V. PROPOSED WORK

Since SRAM on process variation show increase in leakage current also its area requirement is high as compared to DRAM cell. In conventional DRAM scaling of capacitor is critical job in VLSI. Also these capacitor show leakage and hence it required periodic refresh. Hence the objective of this paper is to design a DRAM without capacitor.

The 3T1D cell shows the scheme of the basic cell. The basis of the storage system is the charge placed in node S, written from BL write line when T1 is activated.

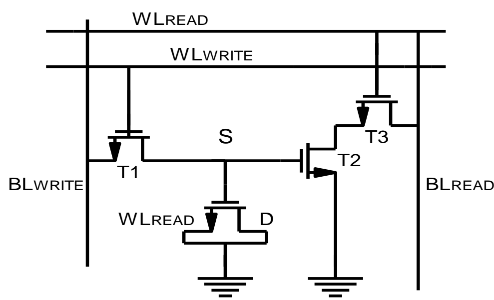

Fig. 1.8 Three Transistor-One Diode DRAM Cell

Consequently, it has a DRAM cell nature, but it allows a non-destructive read process (a clear advantage over 1T1C memories) and a high performance read and writes operation, comparable to 6T SRAM. Transistor T1 and T3 acts as accessing devices, the whole cell is composed by four transistors of similar size to the corresponding of 6T. This implies a more compact cell structure. In order to write the cell at the BL write line level, it is only required to activate T1 through the WL write line. Hence, the S node stores either a 0 or a $Vdd-Vth$ voltage depending on the logic value. This voltage results in the accumulation of charge at the gate of devices D1 and T2. [1]

VI. CONCLUSION

This paper reviews a design method of memory design without capacitor as a storage node. Different SRAM and DRAM design have been discussed on number of transistor required for read/write operation. Also, 3T-1D DRAM cell is an attractive solution to conventional SRAM cell for next generation on chip memory design. We have showed that 3T-1D solves a scaling problem of capacitor in SRAM. This approach provides a comprehensive solution to many of the issues that will impact on-chip memory design in nano scale process technologies.

REFERENCES

1. X. Liang, R. Canal, G. Wei, and D. Brooks "*Replacing 6T SRAMs with 3T1D DRAMs in the L1 data cache to combat process variability*", IEEE Computer Society, Vol.8, No.1:pp.60-68, January-February 2008.
2. B. Raj, A. Suman & G. Singh "*Analysis of Power Dissipation in DRAM Cells Design for Nanoscale Memories*" International Journal of Information Technology and Knowledge Management, Vol. 2, No. 2, pp. 371-374 July-December 2009.
3. M. Tien Chang, P. Tsang Huang and W. Hwang "*A 65nm Low Power 2T1D Embedded DRAM with Leakage Current Reduction*" in 39th IEEE National Science Council and Ministry of Economic Affairs International Symposium on Micro architecture, Vol.1, No.12, pp.56-62, July- December 2006.
4. S. Lin, Y. Kim and F. Lombardi "*A 32nm SRAM Design for Low Power and High Stability*" IEEE Journal of in Solid-State Circuits, Vo. 42, No. 3, pp. 680 - 688, January-March 2007.
5. B. Amelifard, F. Fallah "*Leakage Minimization of SRAM Cells in a Dual-Vt and Dual-Tox Technology*" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 7, Jun-July 2008.
6. N. Bhat " *Design and Modeling of Different SRAM's Based on CNTFET 32nm Technology*" International Journal of VLSI design & Communication Systems, Vol.3, No.1, November-February 2012.
7. N. Bhat " *Design and Modeling of Different SRAM's Based on CNTFET 32nm Technology*" International Journal of VLSI design & Communication Systems, Vol.3, No.1, November-February 2012.
8. B. Davis "*Modern DRAM Architectures*" In Proc. 26th Annual International Symposium on Computer Architecture, Vol.2, No. 26, pp. 222–233, July- December 1999.
9. X. Liang, R. Canal, G. Wei and D. Brooks "*Process Variation Tolerant 3T1D-Based Cache Architectures*" School of Engineering and Applied Sciences, Harvard University, Cambridge, vol. 36, no. 4, pp. 658–665, 2001.
10. S. M. Kang & Y. Leblebici "CMOS Digital Integrated Circuits Analysis and Design" 3rd edition TATA McGraw Hill Edition, pp.405-474

AUTHORS PROFILE

Yogesh N. Thakre received the bachelor's degree in Electronics and Telecommunication engineering from HVPM College of Engineering & Technology, Amravati, Maharashtra, India and currently pursuing M. Tech in Electronic System and Communication from Govt. College of Engineering, Amravati, Maharashtra, India.

Shubhda S. Thakare received the bachelor's and master's degree from Amravati University. Currently she is an Assistant Professor at Government College of Engineering, Amravati, Maharashtra, India with over 14 years of experience in teaching field. Her current areas of research are VLSI and Embedded Systems.

Dr. Devendra S. Chaudhari obtained BE, ME, from Marathwada University, Aurangabad and PhD from Indian Institute of Technology, Bombay, Mumbai. He has been engaged in teaching, research for period of about 25 years and worked on DST-SERC sponsored Fast Track Project for Young Scientists. He has worked as Head Electronics and Telecommunication, Instrumentation, Electrical, Research and incharge Principal at Government Engineering Colleges. Presently he is working as Head, Department of Electronics and Telecommunication Engineering at Government College of Engineering, Amravati. Dr. Chaudhari published research papers and presented papers in international conferences abroad at Seattle, USA and Austria, Europe. He worked as Chairman / Expert Member on different committees of All India Council for Technical Education, Directorate of Technical Education for Approval, Graduation, Inspection, Variation of Intake of diploma and degree Engineering Institutions. As a university recognized PhD research supervisor in Electronics and Computer Science Engineering he has been supervising research work since 2001. One research scholar received PhD under his supervision. He has worked as Chairman / Member on different university and college level committees like Examination, Academic, Senate, Board of Studies, etc. he chaired one of the Technical sessions of International Conference held at Nagpur. He is fellow of IE, IETE and life member of ISTE, BMESI and member of IEEE (2007). He is recipient of Best Engineering College Teacher Award of ISTE, New Delhi, Gold Medal Award of IETE, New Delhi, Engineering Achievement Award of IE (I), Nashik. He has organized various Continuing Education Programmes and delivered Expert Lectures on research at different places. He has also worked as ISTE Visiting Professor and visiting faculty member at Asian Institute of Technology, Bangkok, Thailand. His present research and teaching interests are in the field of Biomedical Engineering, Digital Signal Processing and Analogue Integrated Circuits.