Design & Simulation of CMOS Inverter at Nanoscale beyond 22nm

Adil Zaidi, Kapil Garg, Ankit Verma, Ashish Raheja

Abstract— ***Power and area are the two major concerns in design of any digital circuit. At present scenario low power device design and its implementation have got a significant role in the field of nano electronics. This paper investigates the applications of CMOS technology in the nanometer regime beyond 22 nm channel length where the relative study of average power dissipation of CMOS inverter is found in nano Watts. The simulation results are taken at different channel length (16nm 22nm, 32nm, 45nm) using CMOS technology with the help of (H-spice) simulation tool. The results are analyzed at different supply voltages keeping constant load capacitance (C_{load} =1fF) apart from this, values of various internal parameters of CMOS Inverter at different channel length are calculated.***

Index Terms - Nano-electronics, UDSM (Ultra Deep Sub-Micron) Technology, CMOS, and Scaling.

I. INTRODUCTION

The increasing prominence of portable system and the need to limit power consumption in very high density VLSI chips have led to rapid and innovative development in low-power during recent years [1]. From the last few decades the CMOS technology has emerged as a predominant technology in the field of nano electronics. As the technology has become compact there is rapid increase in demand of high performance and low power digital systems.
CMOS technologies rapidly captured the digital market CMOS gates dissipated power only during switching and required very few devices, two attributes in sharp contrast to their bipolar or GaAs counterparts. It was also soon discovered that the dimensions of MOS devices could be easily scaled down more easily than those of other types of transistors. Furthermore CMOS circuits proved to have a lower fabrication cost. CMOS technology is used due to the low cost of fabrication and possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance so as to reduce the cost of packaging [2]. Since the CMOS inverter does not draw any significant current form the power source in both of its steady state operating points, the DC power dissipation of the circuit is almost negligible. The drain current that flows through the nMOS and the pMOS transistors in both cases is essentially limited to the reverse leakage current of the source and drain pn-junction [1].

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Adil Zaidi Electronics & Communication, CET-IILM-AHL, Greater Noida, Uttar Pradesh, India.
Kapil Garg, Electronics & Communication, CET-IILM-AHL, Greater Noida,, Uttar Pradesh, India.
Ankit Verma, Electronics & Communication, CET-IILM-AHL, Greater Noida,, Uttar Pradesh, India.
Ashish Raheja, Electronics & Communication, CET-IILM-AHL, Greater Noida,, Uttar Pradesh, India.

The design of high density Chips in MOS VLSI technology requires that the packaging density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. Reduction of size i.e. the dimension of MOSFET gets reduced is termed as scaling [3]. With the help of scaling the electrical properties of the MOSFET can be altered and complexity is reduced [4]. Scaling seems to play to play a vital role in enhancing characteristic MOSFET which further leads to low power dissipation and cost per function.
Power consumption has repeatedly been the driving force behind changes in the preferred transistor technology of choice in designing integrated circuits (ICs). Moves from bipolar to nMOS and then nMOS to complementary MOS (CMOS) technologies occurred primarily due to the much lower power consumption [5]. To cope up with the limitations of power dissipation we scale down the dimensions of the transistor since the power delivered is proportional to the square of supply voltage VDD power dissipation occurs due to charging and discharging of load capacitance [6].

$$P = C_L V_{DD}^2 F_d$$

Where
P is the power dissipated,
C_L is the load capacitance,
V_{dd} **is** the power supply voltage and
F_d is the frequency.

The advanced productions of integrated circuits are built on CMOS devices with minimum feature sizes of 40 nm. Here in this paper we are trying to design the CMOS inverter at channel length of 16nm starting from channel lengths 45nm, 32nm, 22nm using H-spice [7]
The paper is classified as follows: section II includes the design & power model of CMOS inverter at nano scale which describes the schematic view of the CMOS INVERTER considering its power dissipation factor. Section III describes simulated characteristics i.e. D.C and Transient curves at NANO SCALE. Section IV includes results and discussion, Section V contains acknowledgement followed by references in section VI.

II. DESIGN & POWER MODEL OF CMOS INVERTERAT NANO SCALE

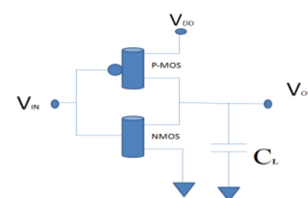

FIGURE 1. CMOS INVERTER

A. DESIGN

MOSFETs are continuously scaled to smaller dimensions to reduce the space complexity. UDSM (Ultra Deep Sub-Micron) Technology deals with MOS devices with channel length in the order of 0.25µm to 0.022µm or even less. The integration of nanostructures at room temperature smaller than 10nm is far too sensitive to size variations of even a few atomic widths [8]**.** Here the CMOS inverter is designed at different nano scales as mentioned and the values of different parameters are also calculated as mentioned in the table 1.The CMOS inverter is shown in figure 1

B. POWER MODEL OF CMOS INVERTER

Three types of power dissipation occur in CMOS inverter circuits, which are given below:

(i) Leakage power Dissipation: In OFF-state, the main components of leakage currents are sub-threshold leakage (Isub), gate induced drain leakage (IGIDL), gate tunnelling leakage (IGATE) and band-to-band tunnelling (IBTBT).

(ii) Short-circuit Power: From the α-power law [9] the short circuit power dissipation model is

$$P_{Sht_ckt_pw} = V_{DD} t_T I_{DO} \frac{1}{\alpha+1} \frac{1}{2^{\alpha-1}} \frac{(1-2v_T)^{\alpha+1}}{(1-v_T)^{\alpha}}$$

$$Where \quad v_T = \frac{V_{TH}}{V_{DD}}$$

III. DYNAMIC POWER OR SWITCHING POWER:

This type of power dissipation occurs due to the charging and discharging of load and parasitic capacitors. Dynamic power expression indicate that the average dynamic power of a complex gate due to the output load capacitance.

$$P_{dynamic} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f + \sum_{i=1}^{n} \alpha_i \cdot C_i \cdot V_{DD} \cdot (V_{DD} - V_T)$$

Dynamic power expression indicate that the average dynamic power of a complex gate due to the output load capacitance [8].

Where,

C_L=Load Capacitance,

Vdd=Supply Voltage,

f=Operating Clock Frequency and

α → switching activity of gate (the probability of a 0-1 switch in a cycle)

Here in this paper we focussed to analyse the average dynamic power or switching power.

IV. SIMULATED CHARACTERISTICS

The dc and voltage transient characteristics as obtained for CMOS inverter using H-SPICE simulator tool at different channel lengths viz. 45nm, 32nm, 22nm, 16nm are shown below.

A. VOLTAGE-TRANSIENT CHARACTERISTICS

Shows input voltage Shows output voltage

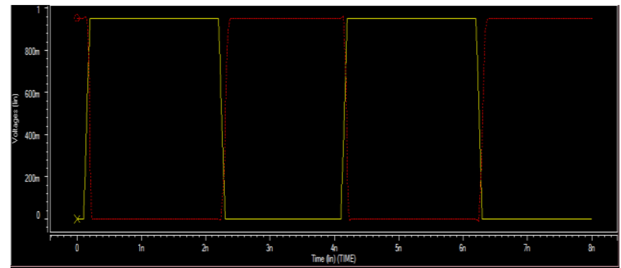

FIGURE 2(a): FOR 45nm

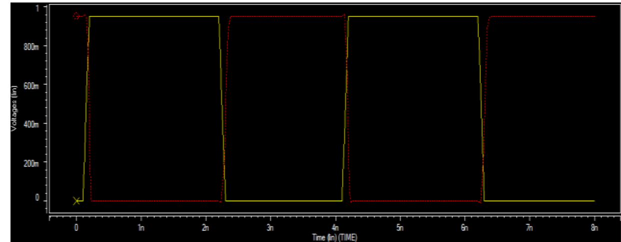

FIGURE 2(b): FOR 32nm

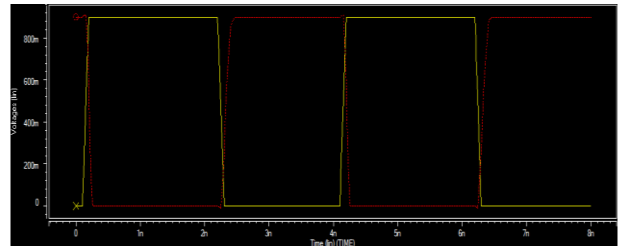

FIGURE 2(c): FOR 22nm

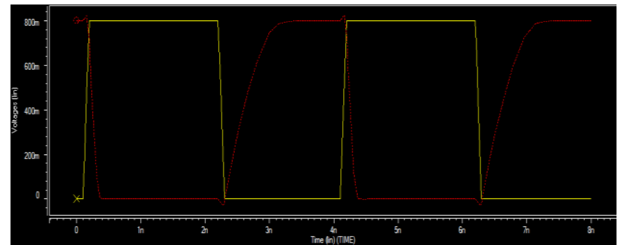

FIGURE 2(d): FOR 16nm

B. DC CHARACTERISTICS

Shows input voltage Shows output voltage

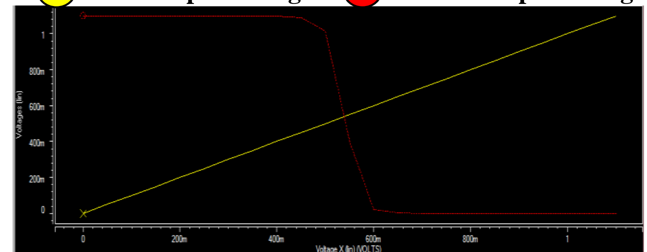

FIGURE 3(a): FOR 45nm

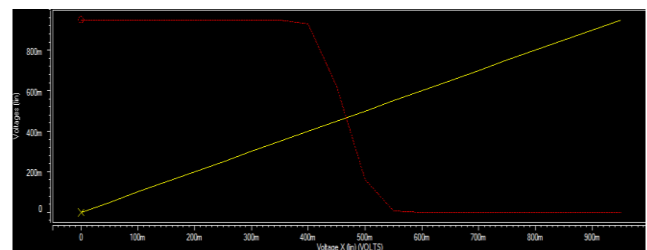

FIGURE 3(b): FOR 32nm

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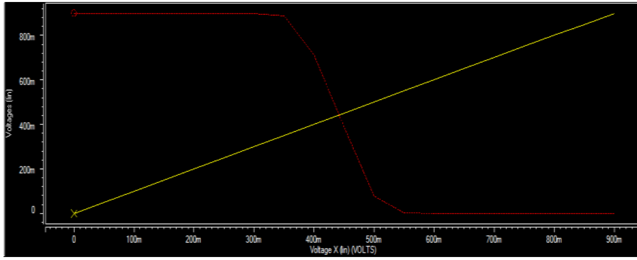

FIGURE 3(c): FOR 22nm

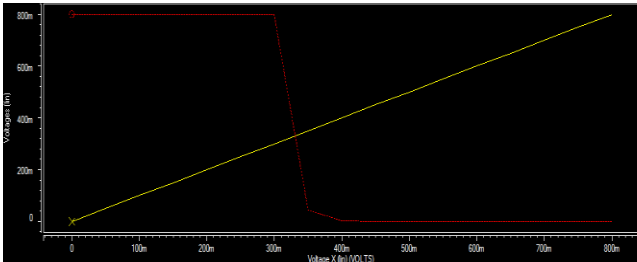

FIGURE 3(d): FOR 16nm

C. INTERNAL PARAMETERS

The various internal parameters mentioned in TABLE 1 are
Currents: I_d, I_{bs}, I_{bd}.
Voltages: V_{gs}, V_{ds}, V_{bs}, V_{th}, V_{od}, V_{dsat}.
Transconductances: g_m, g_{ds}, and g_{mb}.
Capacitances: C_{gd}, C_{gtot}, C_{stot}, C_{btot}, C_{gs}, C_{dtot}
Other: Region of operation and Beta.

In the above parameters the various subscripts shown indicates:
g for gate terminal
d for drain terminal
s for source terminal
b for body or substrate
tot for total
th for threshold
o for output
Parameters
The parameters shown below are for different values of channel length viz. 45nm and 32nm.

TABLE2: VALUES AT 22nm & 16nm

CHANNEL LENGTH	At 45 nm		At 32 nm	
PARAMETER	NMOS	PMOS	NMOS	PMOS
Region	Cut-off	Linear	Cut-off	Linear
I_d	-3.0736p	6.1367p	-2.40p	7.3002p
I_{bs}	-1.1000p	4.58e-20	-950.0075f	8.936e-20
I_{bd}	1.433e-24	-6.663e-26	1.237e-24	-1.774e-26
V_{gs}	-1.1000	-1.1000	-949.999m	-949.999m
V_{ds}	-1.1000	45.8505n	-949.999m	89.3335n
V_{bs}	-1.1000	45.8505n	-949.999m	89.3335n
V_{th}	555.2204m	-587.69m	545.2582m	-581.274m
V_{dsat}	41.5588m	-378.97m	43.4974m	-318.774m
V_{od}	-1.6552	-512.30m	-1.4953	-368.72m
Beta	1.5772m	359.213u	1.3938m	290.27u
g_m	82.0249p	7.5330p	64.3262p	14.4414p
g_{ds}	5.5889p	133.840u	6.1920p	81.7185u
g_{mb}	24.0493p	2.3834p	18.9437p	4.0645p
C_{dtot}	117.3034a	151.079a	80.3333a	99.4252a
C_{gtot}	111.4480a	233.366a	69.5154a	140.2455a
C_{stot}	116.3603a	259.622a	81.8091a	167.9399a
C_{btot}	181.5563a	199.240a	126.3500a	138.2493a
C_{gs}	31.8388a	103.563a	20.2244a	59.8354a
C_{gd}	49.9393a	127.6948a	32.4299a	78.4655a

TABLE1: VALUES AT 45nm & 32nm

CHANNEL LENGTH	At 22 nm		At 16 nm	
PARAMETER	NMOS	PMOS	NMOS	PMOS
Region	Cutoff	Linear	Cutoff	Linear
I_d	900.3907f	14.2695p	-55.8398f	68.0084p
I_{bs}	-900.004f	3.45e-19	-800.0022f	5.4164a
I_{bd}	1.172e-24	-1.54e-26	1.042e-24	-1.789e-26
V_{gs}	-899.99m	-899.999m	-799.9946 m	-799.9946 m
V_{ds}	-899.99m	345.4881n	-799.9946 m	5.4148u
V_{bs}	899.99m	345.4881n	-799.9946 m	5.4148u
V_{th}	569.3693 m	-631.84m	648.4954m	-686.8784 m
V_{dsat}	42.4761m	-258.108 m	43.6988m	-130.6667 m
V_{od}	-1.4694	-268.15m	-1.4485	-113.1162 m
Beta	1.1252m	192.0729u	861.5537u	142.7162u
g_m	24.0010p	46.9263p	1.5064p	679.5415p
g_{ds}	3.5404p	41.3023u	80.9335f	12.5595u
g_{mb}	7.1595p	11.4772p	469.9976f	142.7086p
C_{dtot}	53.0946a	63.8123a	77.8653a	102.4234a

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C_{gtot}	41.7833a	80.9348a	72.3080a	136.6849a
C_{stot}	54.9811a	104.4578a	81.3225a	153.8557a
C_{btot}	84.9796a	92.9971a	135.3761a	142.2724a
C_{gs}	12.2789a	32.9790a	18.0982a	53.1671a
C_{gd}	12.2789a	32.9790a	29.9621a	77.7244a

V. RESULTS & DISCUSSIONS

The simulated dc and ac characteristics shown in FIGURE 2 & 3 depicts the variation of input voltage with respect to output voltage and variation of output voltage with respect to time (time domain approach) respectively which help us to find out the average power dissipated at various channel length maintaining the different power supply as mentioned in the TABLE 3

TABLE3: AVERAGE POWER DISSIPATED WITH CHANNEL LENGTH

Channel Length (nm)	Optimum Supply Voltage (volts)	Power dissipation (NanoWatts)
45	1.1	398
32	0.95	241.6
22	0.9	238
16	0.8	215

The figure 4 shows the variation of average power dissipated with respect to the channel length in nano scale based on the values mentioned in TABLE3. The graph clearly shows as the channel length is decreasing following the sequence, 45 nm, 32 nm, 22nm & 16 nm, the average power dissipated is also decreasing following a exponentially decaying curve thus the components density can be increased in a small area with an effective decrease in average power dissipation .Finally the CMOS inverter is designed at a nano scale of channel length 16nm with power supply of 0.8 volts will improve the power dissipation factor. Further the values of various internal parameters are presented in TABLE 1 & 2.

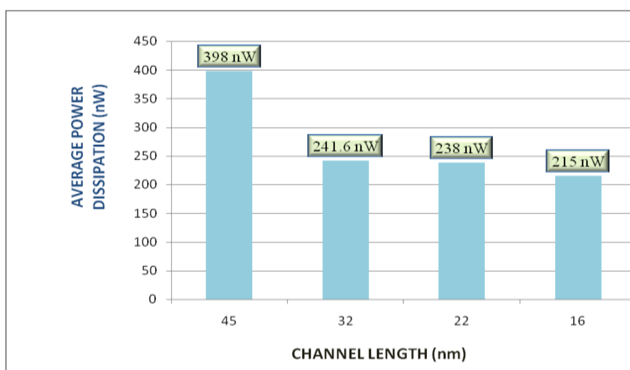

FIGURE 4: Variation of average dissipated power with channel length

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AUTHORS PROFFILE

Adil Zaidi has received his Bachelors Degree B.Tech in Electronics and Communication from CET-IILM-AHL, Greater Noida, and Master's Degree M.Tech in VLSI Design from Maharishi Dayanand University, Haryana. His research interest includes Analog & Digital VLSI Design, Low Power Circuits, CNTFET, Nanoelectronics etc. Presently he is serving as Assistant Professor in the Department of Electronics and communication Engineering, CET-IILM-AHL, Greater Noida Uttar Pradesh, India.

Kapil Garg is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had undergone training from National Physical Laboratory; Delhi. He had done paper presentations on Defected Ground Structure [DGS].He is researching on reduction of power dissipation and area in CMOS technology at Nanoscale.

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Ankit Verma is pursuing B.TECH from CET-IILM –AHL, Greater Noida in Electronics and Communication engineering. He had undergone summer training with DMRC (Delhi metro rail corporation) and Rooman Technologies in summer 2012. During his research he worked in the field of VLSI technology on HSPICE simulation tool *in order to reduce* the power dissipation and area at Nanoscale

Ashish Raheja is pursuing B.TECH from CET-IILM-AHL, Greater Noida in electronics and communication engineering. He was an intern with DMRC (Delhi metro rail corporation) in summer of 2012 .His research interest includes design of low power circuits using Nanoscale CMOS so as to reduce power dissipation and area .

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