Design of Low Power Phase Frequency Detectors for Delay Locked Loop

Raj Nandini, Himadri Singh Raghav, B.P.Singh

Abstract— A simple new Phase Frequency Detector design is presented in this paper. The PFD which helps Delay Locked Loop (DLL) to achieve simultaneous phase and frequency error detection is an indispensable block and plays an important role in improving the performance of the whole DLL system. Both conventional and improved PFDs are implemented using tanner 0.18 µm CMOS Process. The layouts are also designed using Tanner Tool. The maximum frequency of operation is 1 GHz when operating at 1.8V voltage supply. It can be used in DLL for high speed and low power consumption applications.

Index Terms— CMOS Integrated Circuits, Delay Locked Loop, Phase Frequency Detector, Tanner

I. INTRODUCTION

A dynamic de-skew circuit can be used to ensure good clock alignment across variations in process, voltage and temperature (PVT). The DLL is such a circuit, using a first-order closed-loop architecture that dynamically aligns its output clock signal with a reference clock signal. DLLs are widely employed in microprocessors and memory interfaces to eliminate clock skew [1]. They can also be used to generate multiple clock signals on chip for applications such as for Built In Self Test (BIST) circuits. In general DLL consists of four main blocks.

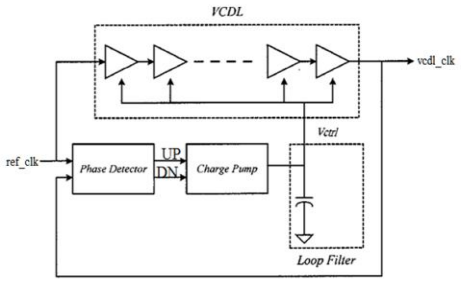

Fig1 DLL Block Diagram

1.Phase Detector or Phase Frequency Detector(PD or PFD)
2.Charge Pump(CP)
3.Loop Filter
4.Voltage Controlled Delay Line(VCDL)

In a DLL, the input clock signal propagates through the Voltage Controlled Delay Line and develops phase shift (or time delay) at every delay stage of the VCDL. The phase shift of each delay stage is controlled by the voltage of a loop filter. The output is taken from one of the delay stages. The phase of the output signal is compared with the phase of the input signal in the Phase Detector. The phase error information generated by PD (usually in the form of voltage or a current) is transferred to the Charge Pump . The CP uses the phase error information to adjust the voltage of the loop filter and thus to change the delay of the VCDL. Owing to such a negative feedback mechanism, the phase error is gradually reduced until it finally becomes zero. At that time, the delay of whole VCDL line becomes equal to one clock cycle and the voltage of the loop filter is utilized, which indicates that a locked state has been established [2].

II. CIRCUIT DESCRIPTION

A. PFD using NOR GATE

Fig 2 shows the block diagram of PFD using NOR gate. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NOR Gate in the reset path [3]. The inputs REF and VCDL serve as clocks of the flip flops. At any point of time, the PFD can be in one of the four states:

- UP=0 and DN=0
- UP=1 and DN=0
- UP=0 and DN=1
- UP=1 and DN=1

The UPb and DNb signals are given as input to the NOR gate. Suppose the rising edge of REF leads that of VCDL, then UPb goes to logic low i.e. UP keeps high until the rising edge of VCDL makes DNb on low level. Because UPb and DNb, are NORed, so RESET goes to logic high and resets the PFD into the initial state.

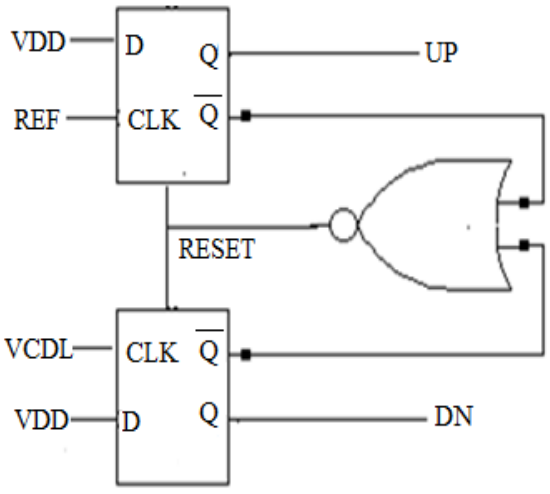

Fig 2 Block Diagram of PFD using NOR gate

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B. NOR Gate using different styles

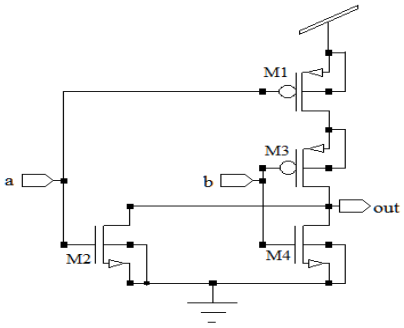

Fig. 3 The Basic Structure of Two-Input CMOS NOR gate

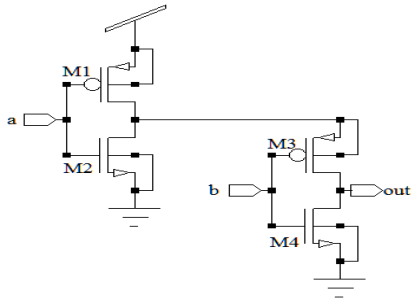

Fig. 4 The Basic Structure of Two-Input GDI NOR gate

C. *Schematics of PFDs*

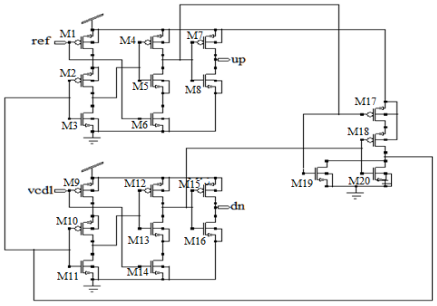

Fig 5 Schematic of Conventional PFD using CMOS NOR gate

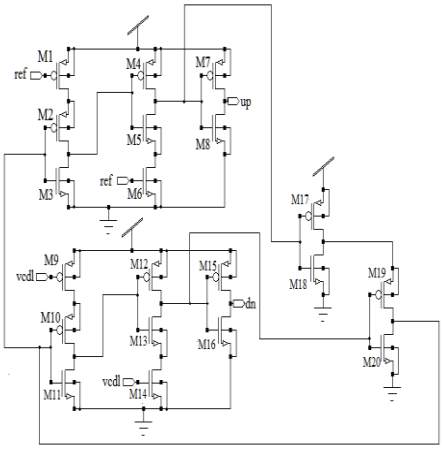

Fig 6 Schematic of Improved PFD using GDI technique NOR gate

D. Layouts of PFDs

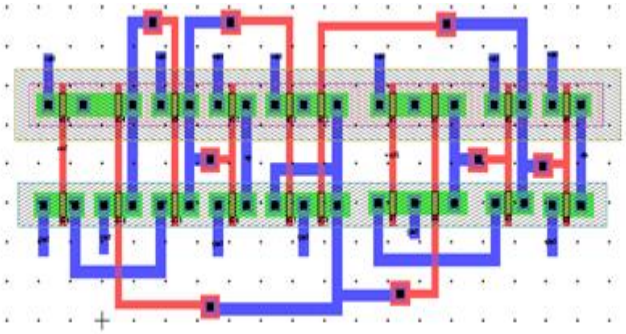

Fig 7 Layout of Conventional PFD using CMOS NOR gate

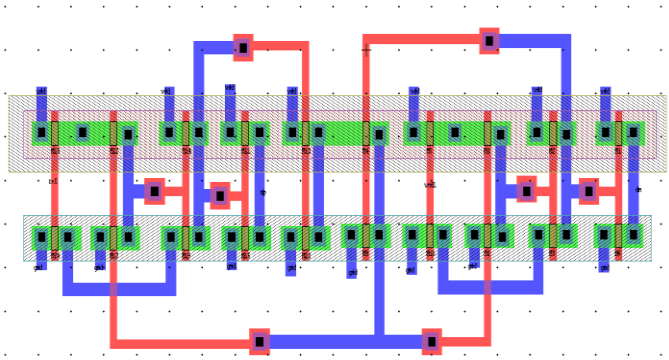

Fig 8 Layout of Improved PFD using GDI technique NOR gate

III. SIMULATION RESULTS

A. *Output Waveforms*

The phase frequency detector circuit can be analyzed in three different ways. One way in which ref signal leads vcdl signal, second in which ref signal lags vcdl signal and third ref signal is in phase with vcdl signal. In the first case, ref signal is leading vcdl signal. In this up pulse represents the difference between the phases of two clock signals.

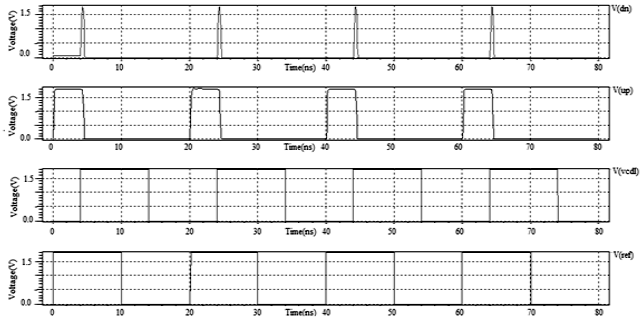

Fig 9 PFD simulation I (ref signal leads vcdl signal)

In the second case, ref signal is lagging vcdl signal. In this dn pulse represents the difference between the phases of two clock signals.

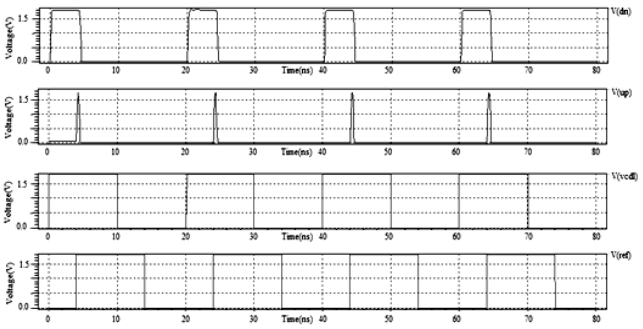

Fig 10 PFD simulation II (ref signal lags vcdl signal)

In the third case, ref signal is in phase with vcdl signal. In this case, the loop is in locked state and short pulses will be generated on the up and dn outputs.

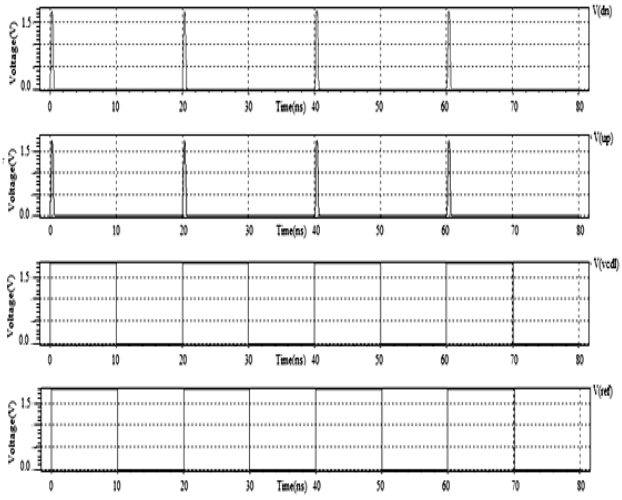

Fig 11 PFD simulation III (ref signal is in phase with vcdl signal)

B. Performance Comparison

Table I depicts different parameters for the conventional PFD and Improved PFD for various parameters.

TABLE I: COMPARATIVE ANALYSIS OF PFDS

Parameters	PFD using GDI NOR Gate (Improved)	PFD using CMOS NOR Gate (Conventional)
Max. Operating Frequency	1 GHz	1 GHz
Power Consumption(Watts)	1.869294e-005	2.912547e-005
Glitch Period	5.25ns to 5.52ns	5.12ns to 5.66ns
Glitch Time	270ps	540ps
Transistor Counts	20	20
Supply Voltage	1.8v	1.8v
Delay(sec)	5.4356e-009	5.6597e-009

IV. CONCLUSION

This paper presents two PFD designs implemented in 180 nm CMOS process. The power consumption, glitches and delay of improved PFD using GDI based NOR gate shows advantages compared to the conventional PFD using CMOS based NOR gate. Operating frequency remains the same for the two PFDs.

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