High Performance SiGe Power HBTs for Portable Microwave Applications

L. Megala, B. Devanathan

Abstract*— SiGe bipolar technology has matured to provide a less expensive alternative to III-V, while at the same time ensuring superior performance compared to silicon. SiGe bipolar transistors, due to the lower band gap of SiGe (compared to Silicon), combine high-drift velocities with lower recombination in the base to provide higher forward current gain. This material system is very much perfect for high-power RF applications. SiGe HBTs offer important potential advantages over HFETs in terms of high transconductance, controlled linearity, freedom from surface trapping effects and controllable tradeoff of between unity current gain cut-off frequency (f_t) and breakdown voltage. For high power applications, higher breakdown voltage and f_t is necessary. Thus SiGe material system will have superior performance over other material systems. In this paper, we analyze the performance of SiGe HBTs for analog/RF applications. Improvements in terms of early voltage, intrinsic gain and junction breakdown voltage are noticed. Moreover f_t and f_{max} for these devices show significant improvement making these devices an able candidate for future RF applications. SiGe HBT has been developed and verified by means of TCAD simulation.

***Index Terms*- SiGe HBTs, HFETs, cut-off frequency, breakdown voltage, transconductance.**

I. INTRODUCTION

The **heterojunction bipolar transistor (HBT)** is an improvement of the bipolar junction transistor (BJT) that can handle signals of very high frequencies up to several hundred GHz. It is common in modern ultrafast circuits, mostly radio frequency (RF) systems, as well as applications requiring a high power efficiency, such as power amplifiers in cellular phones.

HBTs can provide faster switching speeds than silicon bipolar transistors mainly because of reduced base resistance and collector-to-substrate capacitance. HBT processing requires less demanding lithography, cost less to fabricate, provide higher breakdown voltages and easier broad-band impedance matching than GaAs FETs. In comparison with Si bipolar junction transistors (BJTs), HBTs show better performance in terms of emitter injection efficiency, base resistance, base-emitter capacitance and cutoff frequency.

Heterojunction Bipolar Transistor has a great potential for high speed applications. HBT devices, particularly SiGe HBTs are efficient alternative to III-V HBTs as they offer a number of advantages over their homojunction counterparts. This technology is also being used to develop electronics for space applications because of their excellent analog and radio frequency (RF) performance over an extremely wide range of temperatures.

SiGe is the first practical bandgap engineered silicon device. Due to the high speed performance and mature silicon process, SiGe Heterojunction Bipolar Transistor (HBT) has emerged as the technology of the choice for RFICs. The use of a narrow band gap material for the base region results in extremely high values of the emitter efficiency and introduces an additional degree of freedom in device design.

The GaAs HBTs are used for power amplifiers due to their good linearity and high power density characteristics over the past decades. However, the GaAs based power amplifier modules cannot be integrated on the same chip with the rest of transmission or receiving system which are implemented on a Si-based CMOS or BiCMOS chip. However, SiGe based amplifiers could rectify this main disadvantage. On the other hand, as compared with GaAs, the thermal conductivity of SiGe is three times better as large. Due to SiGe HBTs featuring comparable RF performance to that III-V HBTs and low fabrication cost, SiGe HBTs are emerging as a contender for RF power applications. SiGe HBTs has been increasingly used in power amplifier for its high power, low-cost, good linearity and compatibility with BiCMOS technology.

SiGe bipolar technology has matured to provide a less expensive alternative to III-V, while at the same time ensuring superior performance compared to silicon. In these transistors, controlling the germanium profile in the base and the positions of the base p-n junctions is crucial to achieving enhanced performance. Process simulators must model this accurately. Sentaurus process is well suited to SiGe HBT simulation as it has an advanced set of models that take into account differences in lattice spacing between silicon and SiGe and the resulting stress, as well as the effect of germanium concentration on dopant diffusions.

Consequently, understanding device physics of SNWTs and developing TCAD (Technology Computer Aided Design) tools for SNWT design become increasingly important. The *principle objective* of the thesis is to design a Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) using TCAD sentaurus simulation and to obtain the characterization of bipolar transistors. For bipolar transistors, the following simulations are performed: Gummel plots, a family of I_c-V_{cc} curves, junction breakdowns and frequency analysis. This TCAD simulation template has been designed and verified using TCAD Sentaurus Version D-2010.03. The SiGe device structure is created with Sentaurus structure Editor. The Sentaurus workbench template setup can also be used to investigate the electrical properties of device structures created by the process simulator Sentaurus process.

Manuscript received on April, 2013.

L.Megala, Assistant Professor/ECE, V.R.S college of Engineering & Technology, Arasur, Villupuram District, Tamilnadu, India.

B.Devanathan, Lecturer/ECE, University college of Engineering, Kakuppam, Villupuram, Tamilnadu, India.

In this case, Sentaurus process must be added to the tool flow and its input file would need to be adapted to remesh the simulated structure. For each of the simulated I-V curves, relevant electrical parameters such as DC current gain, the Early voltage, the junction breakdown voltages, f_t and f_{max} are extracted. All simulations are performed using the Hydrodynamic transport model, where the carrier temperature equation for the dominant carriers – electrons for the n-p-n transistors and holes for the p-n-p transistors - is solved together with the electrostatic Poisson equation and the carrier continuity equations.

The first section describes modeling of the SiGe Heterojunction Bipolar transistor (HBT) and discusses some aspects of the device properties. It is intended to serve as a starting point for analysis of the SiGe HBT along the procedure mentioned earlier. In the second section, the characterization of bipolar transistors is obtained and some properties of the device are discussed in an analytical approach. The third section presents a numerical example of the other device properties of the SiGe HBT based on the realistic sub-band parameters. The fourth section is the conclusion.

II. DEVICE PROPERTIES

Bipolar transistors remain the primary choice of high frequency power applications due to the high f_t's and high transconductances, g_m. Compared to FET devices, bipolar and devices can maintain high f_t's and g_m's at larger lateral dimensions. Larger lateral dimensions allow for better device matching, critical for microwave/analog circuit design.

The heterojunction bipolar transistor (HBT) is an improvement of the bipolar junction transistor (BJT) that can handle signals of very high frequencies up to several hundred GHz. It is common in modern ultrafast circuits, mostly radio-frequency (RF) systems, as well as applications requiring a high power efficiency, such as power amplifiers in cellular phones. The idea of employing a heterojunction is as old as the conventional BJT, dating back to a patent from 1951.

Homojunction bipolar transistors-BJTs made of one type of material- have fundamental device limitations that do not allow high gain and low base resistance. Schokley and kroemer, in the 1950s developed a way of overcoming constraints of homojunction bipolar transistors by intentionally using two different materials. The technique of changing the bandgap across a device allows for engineering of forces on electrons and holes separately. Taking advantage of GaAs-based techniques that have been refined since the 1970's InP-based HBT's are becoming the popular choice for next-generation high-performance microwave devices. InP utilizes the techniques developed in the GaAs processes to launch another revolution of High speed devices.

The principal difference between the BJT and HBT is in the use of differing semiconductor materials for the emitter and base regions, creating a heterojunction. The effect is to limit the injection of holes from the base into the emitter region, since the potential barrier in the valence band is higher than in the conduction band. Unlike BJT technology, this allows a high doping density to be used in the base, reducing the base resistance while maintaining gain. In 1982 the efficiency of the device was reviewed by Herbert Kroemer, who received a Nobel Prize for his work in heterojunctions in 2000 at the University of California, Santa Barbara.

Materials used for the substrate include silicon, gallium arsenide, and indium phosphide, while silicon / silicon-germanium alloys, aluminium gallium arsenide / gallium arsenide, and indium phosphide / indium gallium arsenide are used for the epitaxial layers. Wide-bandgap semiconductors are especially promising, e.g. gallium nitride and indium gallium nitride.

In SiGe graded heterostructure transistors, the amount of germanium in the base is graded, making the bandgap narrower at the collector than at the emitter. That tapering of the bandgap leads to a field-assisted transport in the base, which speeds transport through the base and increases frequency response.

Heterojunction bipolar transistors have many potential advantages over homojunction bipolar transistors;

- Higher emitter injection efficiency due to larger hole energy barriers in the valence band
- Lower base resistance since the base can be heavily doped without decreasing the emitter injection efficiency
- Less current crowding in the emitter because of a lower voltage drop across the base-emitter junction.
- Improved frequency response due to higher current gain and lower base resistance.
- Wider temperature operation range due to large bandgap (high temperature) and very shallow impurity doping levels (low temperature)

SiGe HBTs offer important potential advantages over HFETs in terms of high transconductance, controlled linearity, freedom from surface trapping effects and controllable tradeoff of between unity current gain cut-off frequency (f_t) and breakdown voltage. SiGe bipolar transistors, due to the lower band gap of SiGe (compared to Silicon), combine high-drift velocities with lower recombination in the base to provide higher forward current gain.

III. SiGe HBT

SiGe bipolar technology has matured to provide a less expensive alternative to III-V, while at the same time ensuring superior performance compared to silicon. SiGe bipolar transistors, due to the lower band gap of SiGe (compared to Silicon), combine high-drift velocities with lower recombination in the base to provide higher forward current gain.

In these transistors, controlling the germanium profile in the base and the positions of the base p-n junctions is crucial to achieving enhanced performance. Process simulators must model this accurately. Sentaurus process is well suited to SiGe HBT simulation as it has an advanced set of models that take into account difference in lattice spacing between silicon and SiGe ant the resulting stress, as well as the effect of germanium concentration on dopant diffusions.

It is assumed that the user is familiar with the sentaurus tool suite, in particular sentaurus Workbench, sentaurus Process, sentaurus Device and Inspect. The focus of this project is to provide a setup that can be used as is or adapted to specific needs. The documentation focuses on aspects of the setups.

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

Sentaurus Process:
The tool sequence for this project starts with sentaurus process, which generates the SiGe HBT devices. Sentaurus process uses the following sentaurus Workbench parameters: collector, base, SiGe_Depo, SIC, Spacer, RTA, and contacts are logical parameters that are used to split the process flow into separate groups of simulation steps that are executed individually. At the end of each group, the current state of the simulated structure as well as the current Sentaurus process are saved and reloaded at the beginning of the next group. This approach allows:

- Easy access to the intermediate structures for verification.
- For split variations. For example, Simulations for different SiGe deposition conditions can be performed without having to re-simulate the processings steps before the SiGe deposition.

Sentaurus Device and Inspect:
Sentaurus Device Simulates Gummel plot curves for the HBT. Relevant electrical parameters, here the DC gain, are extracted with Inspect.

Tool-Specific Setups:
Sentaurus Process:
The process simulations were performed by sentaurus process, which combines advanced SiGe implantation and diffusion models with its meshing engine MGOALS, to obtain accurate and smoothed germanium profiles in the base regions, which are critical to HBT performance.

Process Flow:
The major process steps are:

- Isolation trench definition
- Subcollector Implantation (Split collector)
- Subcollector Activation
- Polysilicon base-contact deposition (Split base)
- Definition of base opening
- SiGe base deposition (Split SiGe_Depo)
- Collector implantation (Split STC)
- Nitrate spacer definition (Split Spacer)
- Final anneal (Split RTA)
- Metallization (Split Contacts)

The process flow is separated into groups of simulation steps. The split points are indicated in the above steps, and the associated Sentaurus Workbench logical parameters are given.

Unified Coordinate System:
Starting with Version D-2010.03, the Unified Coordinate System (UCS) can be activated by using the following command in the Sentaurus process command file: math coord. Ucs
As a result, the sentaurus process coordinate system is used in all subsequent tools. In the Sentaurus process coordinate system, the x-axis points down into the device.

Implantation Models:
For each implantation step, default analytic implantation tables were used for computing the as-implanted profiles of the dopants. These tables are the most advanced, with the moments of the dual- Pearson distributions being extracted from Monte carlo Crystal-TRIM simulations.
The distributon of the generated point defects-mandatory for simulating transient-enhanced diffusion (TED) effects in subsequent diffusion steps – is determined using the '+1' model. For calculating the damage to the crystal, the analytic Hobler model, consisting of a Gaussian primary function with exponential tail, was used.

Diffusion Models:
The ChargedPair model was used for all dopants (including germanium) in silicon. Dopant-point defect pairs and unpaired point defects were treated as mobile species, whereas the substitutional dopants were assumed to be immobile. This model is described by three continuity equations: one for interstitals, vacancies, and unpaired dopants . In addition , due to the presence of germanium, two more equations for germanium diffusion and GeB cluster formation were solved. The effect of germanium on dopant diffusivities by reduction of the intrinsic carrier concentration was also taken inti account.

Deposition of Strained SiGe Base:
A 0.2m thick SiGe layer is deposited with:
Deposited material= {Silicon} type= isotropic
Rate = {1.0} time =0.2
Here, the boron profile is defined in two steps. First, the boron concentration is set to 2 x 10^{17} cm^{-3} for x-values less than -0.035 m and to10^{12} cm^{-3} otherwise. Then a concentration of 7.8 x 10^{18} cm^{-3} is added in the interval between -0.055 m and -0.035 m.
A graded germanium profile in the SiGe layer is defined with:
Sel z="-0.6<x && x<-0.02?
(9*x+0.68)*2.0e22: 1e10" name =Germanium Silicon Store
The initial strain profile in the SiGe base region is set with:
Strain_profile species = Germanium silicon
Ratio= {0.1} strain = {0 0.0425}
pdbSetBoolean Silicon mechanics UpdateStrain 1
The strain_profile command defines that the strain at a mole fraction of 0 is Zero and raises linearly to 4.25% at a mole fraction of 1.

Preparing Structures for Device Simulations:
At the end of the process simulation flow, Sentaurus Process prepares the structures for the subsequent device simulations with Sentaurus Device. For this purpose, the substrate depth is limited to 9.5 m by
Transform cut location= 9.5 down
This is performed because, unlike process simulations, a deep substrate is not needed for device simulations. Meshing requirements for process and device simulations are different in nature. For device simulations, the gradients of individual dopant profiles are not of particular interest. It is more useful to refine on the net active doping concentration. For this remeshing,
First all previously defined refinement boxes are removed:
refinebox clear
refinebox !Keep.lines
line clear
Second, the adaptive meshing defaults are altered to suppress refining profiles irrelevant for device simulations:
Pdbset Grid AdaptiveField Refine.Abs.Error 1e37
Pdbset Grid AdaptiveField Refine.Rel.Error le10
Pdbset Grid AdaptiveField Refine.Target.Length 100.0
Pdbset Grid Adaptive 1
The meshing engine is configured to create high quality mesh elements best-suited for device simulations:
Pdbset Grid SnMesh Delaunytype boxmethod

To activate new refinements, a grid remeshing step is performed:
Grids remesh
Device Simulation using Sentaurus Device, and Extraction and Visualization with Inspect:
Sentaurus Device is used to simulate a Gummel plot for the SiGe HBT. Inspect is used to extract the DC current gain.

Characterization of Bipolar Transistors
For bipolar transistors, the following simulations are performed: Gummel plots a family of I_c-V_{ce} curves, junction breakdown, and frequency analysis. The template is based on a $Si_{0.84}Ge_{0.16}$ heterojunction bipolar transistor (HBT); however, the project structure and input files can be used for any bipolar transistor with only minor modifications. For each of the simulated I-V curves, relevant electrical parameters such as the DC current gain, the early voltage, the junction breakdown voltages, f_t, and f_{max} are extracted.
This project provides standard templates for the device simulator sentaurus device, which can perform the most common types of simulation used in the characterization and performance assessment of bipolar transistors. It contains three different sentaurus workbench setups:

- A DC characterization setup HBT _DC which performs a Gummel plot simulation and computes a family of I_c-V_{ce} Curves
- A small-signal simulation setup HBT_RF, which computes the cut-off frequencies ft and fmax
- A junction breakdown setup HBT_BV, which computes the collector-base (BVcbo), emitter-base (BVebo) and collector-emitter (BVceo) breakdown characteristics.

All three projects are based on an analysis $Si_{0.84}Ge_{0.16}$ n-p-n and p-n-p device structure, which is created with the sentaraus structure editor. The sentaurus workbench template setup can also be used to investigate the electrical properties of device structures created by the process simulator sentaurus process. In this case, sentaurus process must be added to the tool flow and its input file would need to be adapted to remesh the simulated structure.

Sentaurus Structure Editor:
The analysis bipolar structure is defined with the sentaurus structure editor. This first tool setup is identical for all three projects. Three Sentaurus workbench parameters are used by sentaurus structure editor:

- Type = npn|pnp defines whether an n-p-n or a p-n-p bipolar device is created.
- Xeb[1] defines the germanium mole fraction at the emitter-base interface .It assumes the value 0 and 0.16. You can add or remove value as needed.
- Xbc[1] defines the germanium mole fraction at the collector-base interface .It assumes the value 0 and 0.16. You can add or remove value as needed.

The profile of the germanium mole fraction inside the base is a linear interpolation between the values at the two interfaces.

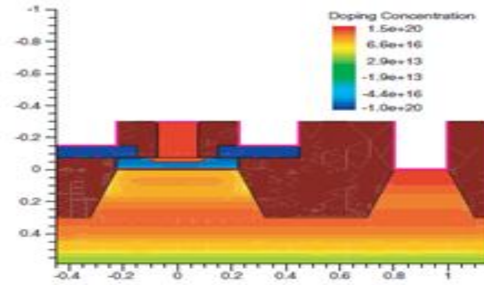

Fig.1 SiGe HBT generated by Sentaurus Structure Editor; concentrations of dopants in various regions are shown.

RF characteristics
For the simulation of the RF characteristics, the same biasing and sweeping scheme as for the gummel plot simulation is used. At each bias point, sentaurus device performs a small-signal analysis for various frequencies and stores the small-signal admittances and capacitances for all contact-to-contact combinations (this data is equivalent to the y-matrix). During post processing with inspect, this data is used to determine the unity current f_t and unity power gain f_{max} frequencies.
A mixed –mode environment is required for AC simulation in sentaurus device, that is, that is instead of simulating an isolated HBT, the HBT is embedded in an external circuit that includes voltage sources attached to each terminal. The circuit connections to the HBT and the voltages and currents to be plotted are defined in the system section:

```
System {
  HBT hbt (base=1 collector=2 emitter=3)
  Vsource_pset vb (1 0) {dc =0}
  Vsource_pset vb (2 0) {dc =0}
  Vsource_pset vb (3 0) {dc =0}
  ACPlot (v(1) v(2) i(vb 1) i(vc 2))
}
```

The solve section is similar to that used for the gummel plot simulation with the addition of an ACCoupled section. At each bias point an AC analysis is performed over a frequency range of 1MHz-100 GHz.

IV.CONCLUSION

High performance characteristics are possible with the introduction of only a very small amount of Si in the emitter region of this Si-Ge/Ge structure. High gain and low forward transit time are possible even with higher doping concentration in the base region than in the emitter region. High performance SiGe power HBTs have been developed and characterized for portable wireless communications at 900MHz. High bias voltage is beneficial to provide excellent power performance of high-power amplification using SiGe HBTs in portable microwave applications. We have shown that SiGe HBTs, which were optimized for high-speed performance in the forward mode of operation, can also exhibit excellent performance in the reverse mode of operation. A regional transit time analysis was performed to study the delay component in the reverse mode. In this paper, some guidelines are provided to improve the device RF performance in this operation mode.

Good low-power performance is obtained as well, which is attributed to a reduction in the device parasitic contributions. The simultaneous availability of a high-speed performance in the forward mode and a low-power performance in the reverse mode offers flexibility to optimize circuit performance in terms of speed, power and area.

REFERENCES

1. N. Zerounian, F. Aniel, B. Barbalat, P.Chevalier, and A. Chantre, "500 GHz cutoff frequency SiGe HBTs," *Electronics Letters,* vol.43, pp. 774-775, July 2007.
2. Z. Xu, G. Niu, L. Luo, P. S. Chakraborty, P.Cheng, D. Thomas, and J. D. Cressler, "Cryogenic RF Small-Signal Modeling and Parameter Extraction of SiGe HBTs," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF'09,* pp.1-4, Jan 2009.
3. S. C. Jain, *Germanium-Silicon Strained Layers and Heterostructures:* Academic Press, Inc. USA, 1994.
4. S. K. MandaI, G. K. Marskole, K. S. Chari, and C. K. Maiti, "Transit time components of a SiGeHBT at low temperature," *Proc. 24th International Conference on Microelectronics,* vol. 1, pp. 315-318, May 2004.
5. Z. R. Tang, T. Kamins, and C. A. T. Salama, "Analytical and experimental characteristics of SiGe HBT with thin u-Si : H emitters," *Solid State Electron.,* vol. 38, pp. 1829-1834, 1995.
6. V. S. Patri and M. J. Kumar, "Profile Design Considerations for minimizing base transit time in SiGe HBT's," *IEEE Tran. on Electron Devices,* vol. 45, pp. 1725-1731, Aug 1998.
7. K. H. Kwok and C. R. Selvakumar, "Profile design considerations for minimizing base transit time in SiGe HBTs for all levels of Injection before onset of Kirk effect," *IEEE Tran. On Electron Devices,* vol. 48, pp. 1540-1549,2001.
8. A. Zareba, L. Lukasiak, and A. Jakubowski, "Modeling of SiGe-base heterojunction bipolar transistor with Gaussian doping distribution," *Solid-State Electron.,* vol. 45, pp. 2029-2032, 2001.
9. H. Kroemer, "Two integral relations pertaining to electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid-State Electron.,* vol. 28, pp. 11011103, 1985.
10. M. Hassan, T. Rahman, and M. Khan, "Analytical Model for Base Transit Time of a Bipolar Transistor with Gaussian-Doped Base," Solid-State Electronics, vol. 50, pp. 327-332, March 2006.
11. R.Lai, et al,. Proceedings of the 2007 IEEE International Electron Devices Meeting, 609 (2007).
12. W.Snodgrass, et al., Procedings of the 2006 IEEE International Electron Devices Meeting, 22.1.1 (2006).
13. W.Snodgrass, et al., Proceedings of the 2007 IEEE International Electron Devices Meeting, 663 (2007).
14. W.Snodgrass, et al., 2008 CS MANTECH Digest of papers, 14.2 (2008).
15. M.Rohner, et al., IEEE Transactions on Electron Devices, 49, 213 (2002).
16. W.R.Eisenstadt, et al., Components', Hybrids, and Manufacturing Technology, IEEE Transactions on 15, 483 (1992).
17. K.Lee, D.H. Cho, K.W.Park, B.Kim, "Improved VBIC Model for SiGe HBTs with a Unified Model of Heterojunction Barrier Effects", IEEE Transactions on Electrons Devices, vol. 53, no.4, 743, 2006.
18. S.M.Sze, Semiconductor Devices, Physics and Technology John Wiley and Sons, Inc 2005, pp.151.
19. A.Guitierrez-Aitken, E.Kaneshiro, B.Tang, J. Notthoff, P. Chin, D. Streit, and A. Oki, B69 GHz frequency divider with a cantilevered base InP DHBT, in IEDM Tech. Dig., 1999, pp.779-782
20. N.D.Aurora, J.R.Houser and D.J.Roulston, "Electron and Hole Mobilities in silicon as a function of Concentration and temperature", IEEE Transactions on Electron Devices, vol.ED29, no.2, pp 292, 1982.

AUTHORS PROFILE

Ms. L.Megala, is an Assistant professor of ECE in V.R.S college of Engineering & Technology. She completed her B.E/ECE in Idhaya Engineering College for women, Chinnasalem in the year 2008. She completed her M.E in the field of Applied Electronics in S.K.P Engineering College, Thiruvannamalai the year 2011. She has attended 5 national conferences and 1 international conference. She is the life time member of ISTE. She has a teaching experience of 2 years. At present, she is going to have a research work in the field of VLSI Design.

Mr. B.Devanathan, is working as a Teaching faculty in University college of Engineering, Villupuram. He completed his B.E/ECE in V.R.S college of Engineering & technology, Villupuram in the year 2007. He did his master degree in the field of Applied Electronics in S.K.P Engineering College, Thiruvannamalai the year 2011. He has attended 4 national conferences and 1 international conference. He has a teaching experience of 3 years. At present, he is going to have a research work in the field of Digital Image Processing.