A Novel Approach for Displaying Data on LCD Directly from PC using FPGA

Neha R. Laddha, A.P.Thakare

Abstract: In traditional microcontroller or micro processor based approach, every LCD display is associated with a static input. This input is static and cannot be changed by user easily as and when needed. Thus restricting the flexibility to user can have in updating the data. In this paper, we propose to design a prototype where we interface UART with LCD display through FPGA board so as to provide flexibility of data which is being displayed directly to LCD. The primary goal is to provide serial communication of keyboard character using USART hyper terminal and display it on HD44780 based LCD controller. This prototype can be further enhanced into single chip which is significance to SOC as ASIC. Thus, this design based Device can prove beneficial for future Consumer Electronics Market. In this design, for serial communication, multi UART with configurable baud rate is implemented. The multi UART and LCD driver are implemented with VHDL language and can be integrated into the FPGA to achieve compact, stable and reliable data transmission. The design has been simulated on ModelSim and implemented using Quartus II on Altera DE1 FPGA board..

Keywords - UART; Asynchronous serial communication; VHDL; Quartus II; ModelSim, Altera DE1 Cyclone II FPGA board.

I. INTRODUCTION

For various electronics application, to display output on output unit, the most preferred LCD display is Hd44780 LCD display [5]. Generally, the HD44780 is interfaced to a microcontroller (μC) or a microprocessor (μP) in order to generate text on the LCD. This is the most cost and time effective implementation since one can easily generate the signals needed in order to write to the LCD simply by writing a program in assembly or other higher level languages, such as C. Also, this task is made even easier with the availability of large amounts of pre-written codes and libraries, allowing hobbyists and engineers to control the HD44780 based Text LCD directly by just calling the function when writing the program.

On the other hand, to interface the HD44780 based LCD to UART through a programmable logic device such as a CPLD or an FPGA would require a design of higher complexity in terms of hardware as opposed to using a microcontroller which is software based.

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Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol; mostly used for short-distance, low speed, low-cost data exchange between computer and peripherals. UARTs are used for asynchronous serial data communication by converting data from parallel to serial at transmitter with some extra overhead bits using shift register and vice versa at receiver. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible. It is generally connected between a processor and a peripheral, to the processor the UART appears as an 8-bit read/write parallel port. Various designs are found in literatures for UART as different systems have different requirements and attributes which require data communication between its functional units. In recent years the researchers have proposed various UART designs like automatic baud rate synchronizing capability[4], predictable timing behavior to allow the integration of nodes with imprecise clocks in time-triggered real-time systems[3], recursive running sum filter to remove noisy samples[1], integration of only core functions into a FPGA chip to ssachieve compact, stable and reliable data transmission to avoid waste of resources and decrease cost[2], programmable logic to enable interfacing between asynchronous communications protocols and DSP having synchronous serial ports.

Hence, in this paper, we propose to design a prototype where we interface UART with LCD display through FPGA board. The primary goal is to provide serial communication of keyboard character using USART hyper terminal and display it on HD44780 based LCD controller. For multi UART, two modules are included; the configurable baud rate and receiver. For LCD Controller, a simple FSM is devised to create a simple controller within the FPGA to output text onto the HD44780 based Text LCD.

II. ALTERA DE1 DEVELOPMENT AND EDUCATIONAL BOARD

Altera DE1 board become one of the most widely development FPGA board which is used to development of FPGA design and implementations. The purpose of the Altera DE1 Development and Education board is to provide the ideal vehicle for learning about digital logic, computer organization, and FPGAs. It uses the state-of the art technology in both hardware and CAD tools to expose researchers and professionals to a wide range of topics. The board offers a rich set of features that make it suitable for research work Altera provides a suite of supporting materials for the DE1 board, including tutorials, “ready-to-teach” laboratory exercises, and illustrative demonstrations [Altera] Figure (1) gives the block diagram of the DE1 board. To provide maximum flexibility for the user, all connections are made through the Cyclone II FPGA device. Thus, the user can configure the FPGA to implement any system design.

The DE1 board features a state-of-the-art Cyclone® II 2C20 FPGA in a 484-pin package. All important components on the board are connected to pins of this chip, allowing the user to control all aspects of the board's operation. For simple experiments, the DE1 board includes a sufficient number of robust switches (of both toggle and push-button type), LEDs, and 7-segment displays. For more advanced experiments, there are SRAM, SDRAM, and Flash memory chips. For experiments that require a processor and simple I/O interfaces, it is easy to instantiate Altera's Nios II processor and use interface standards such as RS-232 and PS/2. For experiments that involve sound or video signals, there are standard connectors for microphone, line-in, line-out (24-bit audio CODEC), SD memory card connector, and VGA; these features can be used to create CD-quality audio applications and video. Finally, it is possible to connect other user defined boards to the DE1 board by means of two expansion headers.

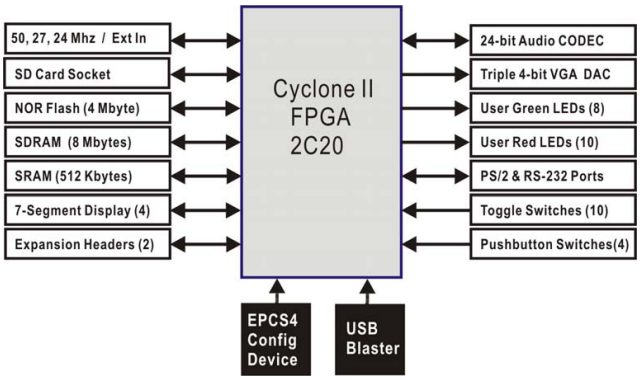

Fig 1. Cyclone II FPGA 2C20

III. IMPLEMENTATION *OF MULTI-UART.*

The UART serial communication module is divided into three sub-modules: the baud rate generator, receiver module and transmitter module, shown in Fig. 1. Therefore, the implementation of the UART communication module is actually the realization of the three sub-modules. The baud rate generator is used to produce a local clock signal which is much higher than the baud rate to control the UART receive and transmit; The UART receiver module is used to receive the serial signals at RXD, and convert them into parallel data; The UART transmit module converts the bytes into serial bits according to the basic frame format and transmits those bits through TXD.

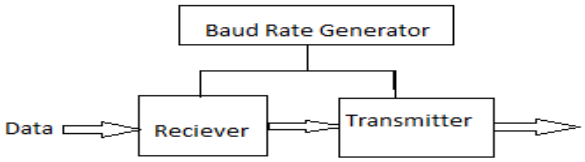

Fig 1.UART Module

A. Baud Rate Generator:

Baud Rate Generator is actually a kind of frequency divider. The baud rate frequency factor can be calculated according to a given system clock frequency and the required baud rate. The calculated baud rate frequency factor is used as the divider factor.

Assume that the system clock is 50MHz, baud rate is 9600bps, and then the output clock frequency of baud rate generator should be 1* 9600Hz.

Therefore the frequency coefficient (M) i.e. counts value of the baud rate generator is:

M =50MHz/1*9600Hz=5208

When the UART receives serial data, it is very critical to determine where to sample the data information. The ideal time for sampling is at the middle point of each serial data bit.

In this design, we designed configurable baud rate generator which can selected by using two switch of cyclone II DE1 board.

S0	S1	Baud Rate(BPS)
0	0	2400
0	1	4800
1	0	9600
1	1	19200
Default		9600

Hence, different baud rate has different frequency coefficient (M) i.e. count value of the baud rate generator.

For 2400Hz, M =50MHz/1*2400Hz=20833

For 4800Hz, M =50MHz/1*2400Hz=10416

For 9600Hz, M =50MHz/1*2400Hz=5208

For 19200Hz, M =50MHz/1*2400Hz=2604

B. Receiver Module:

During the UART reception, the serial data and the receiving clock are asynchronous, so it is very important to correctly determine the start bit of a frame data. The receiver module receives data from RXD pin. RXD jumps into logic 0 from logic 1 can be regarded as the beginning of a data frame.

When the UART receiver module is reset, it has been waiting the RXD level to jump. As we know, the ideal time for sampling is at the middle point of each serial data bit. Hence, RXD low level lasts at least half of receiving clock cycles is considered start bit arrives. Once the start bit been identified, from the next bit, begin to count the rising edge of the baud clock, and sample RXD when counting. Each sampled value of the logic level is deposited in the register parallel_data_signal [7, 0] by order. When the count equals 10, all the data bits are surely received, also the 10 serial bits are converted into a byte parallel data and deposited in the resister parallel_data.

The state machine includes five states: R_Initial (waiting for the start bit), R_Center (find midpoint), R_Delay (Waiting for the sampling), R_Shift register (sampling), and R_Stop (receiving stop bit) is shown in fig 2.

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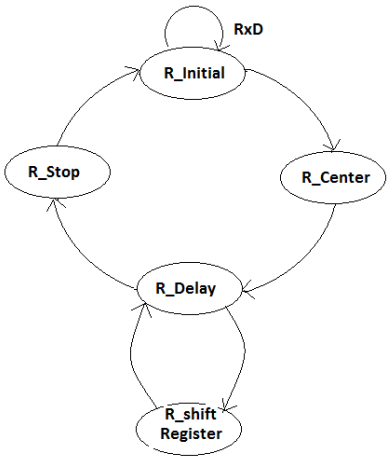

Fig 2. Receiver FSM

R_Initial Status: Initially, the UART receiver is reset; the receiver state machine will be in this state. In this state, the state machine has been waiting for the RXD level to be at logic 0, i.e. the start bit. Start bit indicates the beginning of a new data frame. Once the start bit is identified, the state machine will be transferred to Center state. Also, In this state, start_flag is set to 1.

R_Center Status: For asynchronous serial signal, in order to detect the correct signal each time, and minimize the total error in the later data bits detection. Obviously, it is the most ideal to detect at the middle of each bit. In this state, the task is to find the midpoint of each bit through the start bit. The method is by counting the number of clk_count.

R_Delay Status: When the state machine is in this state, waiting for counting to reach final count value, then entering into shift register to sample the data bits. At the same time determining the received data in 10 bit with start and stop bit.

R_Shift register Status: In this state, data bits are sampled and stored it into shift register which is of 8 bit. After sampling the state machine transfers to delay state unconditionally, waits for the arrival of the next start bit. Also in this state, the start_flag is reset.

R_Stop Status: when stop bit is 1. State machine doesn't detect RXD in stop. After the stop bit, state machine turns back to R_START state, waiting for the next frame start bit.

IV. IMPLEMENTATION OF HD44780 BASED 16X2 LCD DISPLAY MODULE:

For various electronics based projects ranging from hobbyist electronics to industrial based projects, the HD44780 based Text LCD is one of the most preferred choice when it comes to selecting a display output unit.

Typically, the HD44780 is interfaced to a microcontroller (μC) or a microprocessor (μP) in order to generate text on the LCD. This is the most cost and time effective implementation since one can easily generate the signals needed in order to write to the LCD simply by writing a program in assembly or other higher level languages, such as C. The section that follows explains the process that was undergone to produce a FSM using delay elements to accomplish this simple design for interfacing an UART through FPGA to a HD44780 based Text LCD.

A. Interfacing of FPGA pins with 16x2 LCD pin:

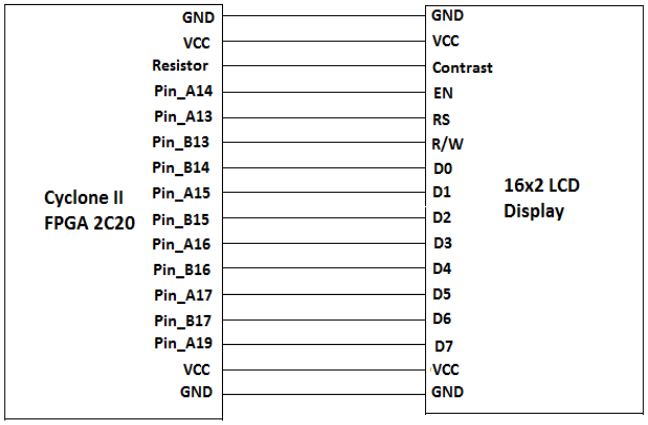

Fig 3. Interfacing of FPGA pins with 16x2 LCD pin

In this design, general purpose input output header pin from Cyclone II DE1 FPGA board are interfaced with Hd44780 LCD display pin. The pin assignment is as shown in fig 3.

B. Initialization of HD44780 LCD Display:

There are two modes of data transfer supported by LCD displays. One is 4bit mode, another is 8 bit mode. In this design we are using 8bit mode. To transfer data In 8 bit mode, first put your data in the 8bit bus, then put command in the command bus and then pulse the enable signal.

To display characters on the 16x2 LCD display, it must be configured first. To configure an LCD display, four command words must be sent to LCD in either 4 bit mode, or in 8 bit mode. The commands are:

1. Function set
2. Display On/Off control
3. Entry mode set
4. Display Clear

The flow chart for data transfer and initialization of LCD display is as shown in fig 4:

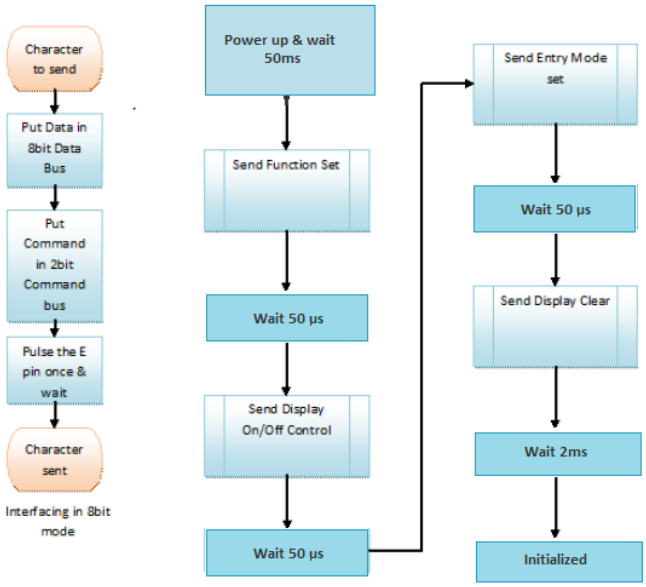

Fig 4. Flow chart for data transfer and initialization of LCD display

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C. Top Model view:

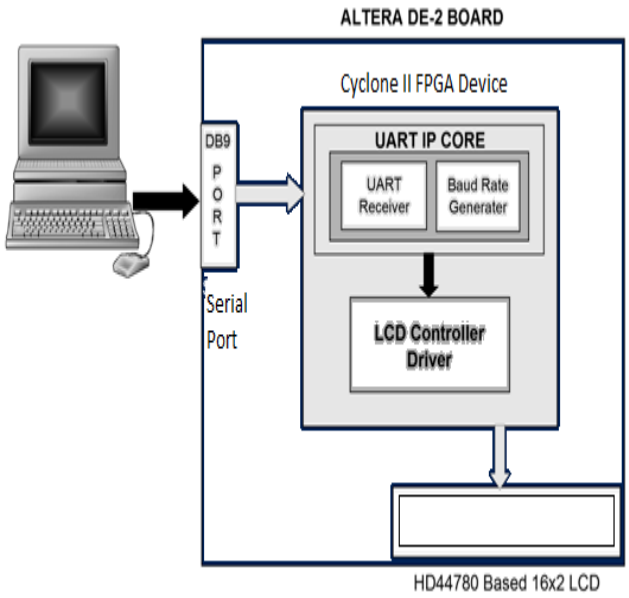


Fig 5. Top Model view

In propose design, there is serial communication of key board characters from USART hyper terminal through USB to serial port FT2302 using UART controller will be display on the HD44780 based 16x2 LCD display using LCD controller

V. SIMULATION *OF MODULES:*

A. UART Simulation:

The simulation is done by using Modelsim Software. The result of simulation is as shown below.

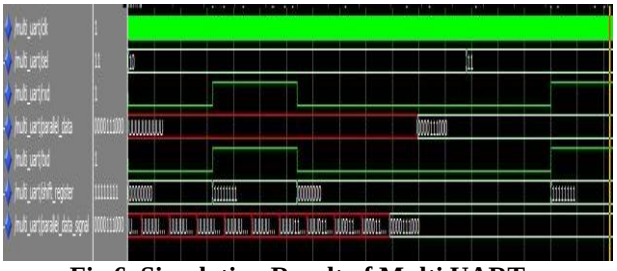


Fig 6. Simulation Result of Multi UART

Fig 6. Shows simulation of UART as a single entity. From simulation waveform, we select baud rate as 19200 using "sel" pin as "11" , as changes happen on "rxd" lines that serial data is stored in shift register and gives parallel data which contains start bit, data bit(8) and stop bit.

B. LCD Controller Simulation:

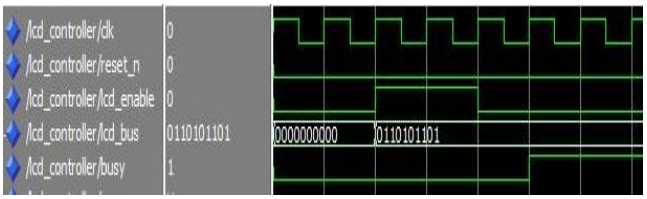


Fig 7. Simulation Result of LCD Controller

Fig 7. Shows simulation of LCD controller. The LCD controller executes an initialization sequence each time it is powered-up or reset_n pin de-asserted for minimum of one clock cycle. The controller asserts the busy pin during initialization. Once initialization completes, the busy pin de-asserts, and the LCD controller waits in ready state for input.

Upon de-assertion of the busy pin, the LCD controller enters the Ready state. We can interface via the lcd_enable and lcd_bus pins to conduct transactions with the LCD module. We initiates this process by issuing the desired data instruction to the lcd-bus and asserting the lcd_enable pin. The LCD controller then asserts the busy pin and manages the transaction. When finished, the de-asserts the busy pin , indicating that it is ready for another instruction. Simulation snapshot depicts the timing diagram for the beginning of transaction.

C. RTL of Top File:

Fig 8. Shows the RTL view of UART Top File. It includes UART modules and LCD Handler Module.

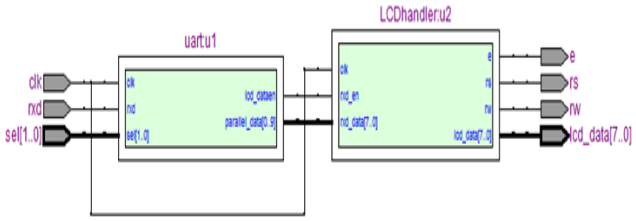
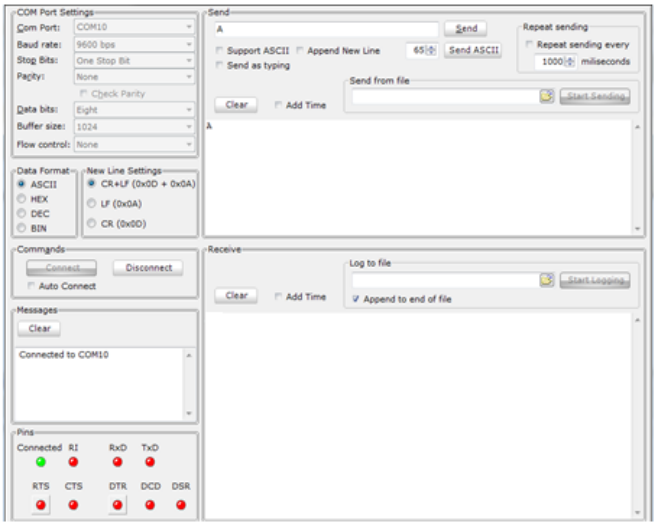
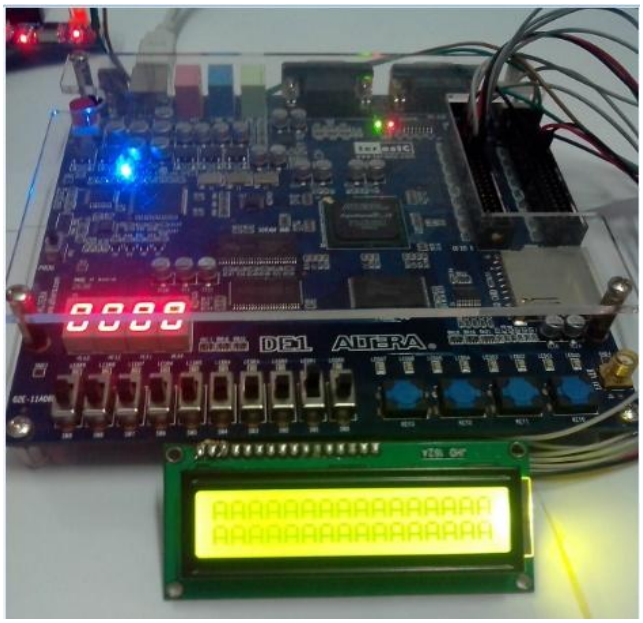


Fig 8. RTL view of Top File

VI. RESULTS

The synthesis is done with Quartus II. After synthesis, code is burn on Altera's DE1 Cyclone II FPGA: EPC215AF484C7 board. In this design instead of using PC hyper terminal, USART hyper terminal of micro C AVR software is used, for any key board character transmission and reception. Considering first input shown below. Here the selected baud rate is 9600 bps to send data 'A'.





Since, the baud rate is 9600 bps; we have to select switch ‘s0’ as “1” & ‘s1’ as “0” which specified that the selected baud rate on Altera DE1 is 9600 bps which means that both baud rate are synchronized. The input data send by USART hyper terminal of micro C AVR software is ‘A’ which as a binary value of 8 bit ‘01000001’. The corresponding output is shown on 16x2 LCD display through FPGA. The output for data is shown in following figure.

VII. CONCLUSION:

Design in this paper is intended to provide more flexibility and to allow dynamic update of data to be displayed on LCD. Prototype implemented for this design uses Multi UART with configurable baud rate, LCD Controller and uses VHDL language to display character on LCD display. This prototype was tested on cyclone II DE1 FPGA board. The design has great flexibility, high integration. Especially in the field of electronic design, where SOC technology has recently become increasingly mature, this design shows great significance.

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