Design of Low Glitch Dynamic Phase Detector for Delay Locked Loop

Shirish Tripathi

Abstract*— A simple Low Glitch Dynamic Phase Detector is proposed in this paper. The Dynamic PD helps Delay Locked Loop to achieve phase error detection in high speed synchronous circuits and plays an important role in improving the performance of the complete DLL block. A high speed, low glitch phase detector is proposed in 180 nm technology with V_{DD}=1.8V in Cadence Schematic Composer for schematic capture, analog artist (Spectre) Tool for simulations and Virtuoso for layouts. The proposed PD is having a better phase sensitivity, phase noise and less power dissipation. Simulation results show that the proposed PD has low glitch as compared to conventional PD based on D flip-flop. So, the speed of the proposed Dynamic PD is also high.

Index Terms*—Delay Locked Loop, Phase Detector, Cadence, CMOS Technology.

I. INTRODUCTION

Delay-Locked Loop (DLL) is a critical circuit component widely used in many timing applications. DLL is a first order loop that compares its input with a reference signal and then delays its output so that it can synchronize with the reference signal in a feedback fashion [1]. The application areas of DLL include clock distribution [2], clock synthesis, memory, microprocessors [3], clock and data recovery, and communication ICs in order to reduce on chip clock buffering delays and improve I/O timing margins.

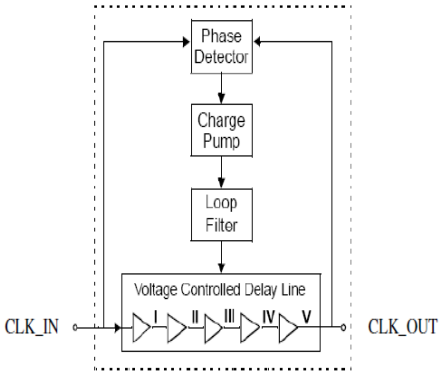

Fig. 1 DLL Block Diagram

A DLL typically basically consists of four basic blocks: a phase detector (PD), a charge pump (CP), loop filter and a voltage-controlled delay line (VCDL). A DLL is essentially a nonlinear negative feedback system. In a DLL, the input clock signal propagates through the VCDL and develops time delay at every delay stage of the VCDL. The phase shift of each delay stage is controlled by the voltage of a loop filter. The output is taken from one of the delay stages. The phase of the output signal is compared with the phase of the input clock in the PD.

The PD generates the phase error information in the form of a voltage or a current which is then assigned to the Charge Pump. The voltage of the loop filter usually known as the control voltage is adjusted by this phase error information which subsequently changes the delay of VCDL. The phase error finally reduced to zero with such negative feedback mechanism. At that time, the delay of the whole VCDL line becomes equal to one clock period, and the voltage of the loop filter is stabilized, which indicates that a locked state has been established [2].

II. CIRCUIT DESCRIPTION

A. PD using D Flip-Flop

The primary objective of the Phase Detector is to measure the phase difference in between the reference and feedback signals. Fig. 2 shows a commonly used flip-flop based linear PD, which consists of two flip-flops and one NAND gate [4]. This Phase Detector consists of two edge-triggered, resettable D flip-flops with their D input held to "1". The inputs CLK_IN and CLK_OUT serve as the clocks for the flip-flops. The outputs of the flip-flops are denoted as UP and DOWN.

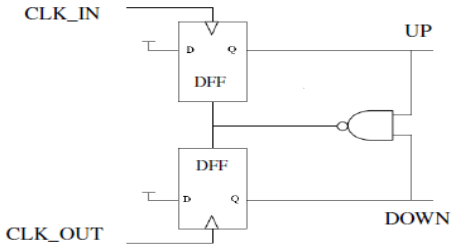

Fig. 2 D Flip-flop based PD

Depending on the operation, the phase detector can be in any of the four states:
a) UP = 0 and DOWN = 0.
b) UP = 1 and DOWN = 0.
c) UP = 0 and DOWN = 1.
d) UP = 1 and DOWN = 1.
However, when both UP = 1 and DOWN = 1 occurs, the AND gate output becomes "1" and both the flips are resetted.

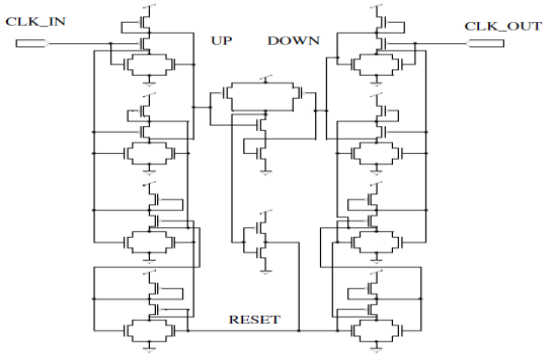

Fig. 3 Schematic of D Flip-flop based PD

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B. Low Glitch Dynamic Phase Detector

The phase detector based on flip-flop has high glitch as compared to dynamic PD. If the glitch is more at the output of PD, the reset time of the flip-flop is also more. Effectively the duration of glitch is a factor which determines the speed of the PD. In order to reduce the glitch as well as increase the speed of PD, a dynamic PD with low glitch is introduced here. The simulation results clearly show that dynamic PD ensures a low glitch in the output as compared to the PD based on flip-flops.

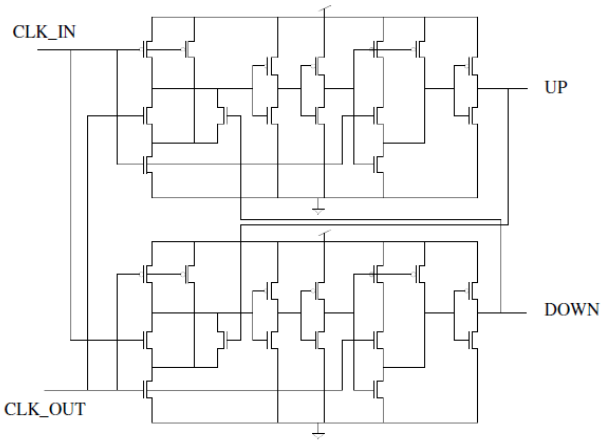

Fig. 4 Schematic of Low Glitch Dynamic PD

C. Layout of Low Glitch Dynamic PD

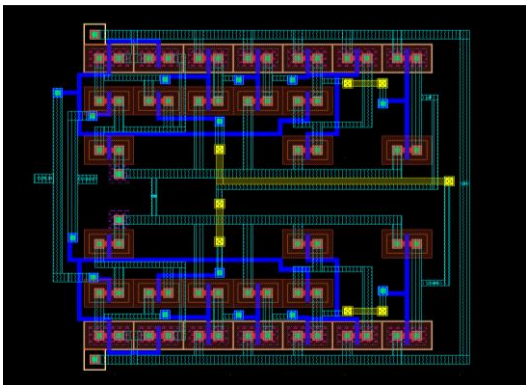

Fig.5 Layout of Low Glitch Dynamic Phase Detector

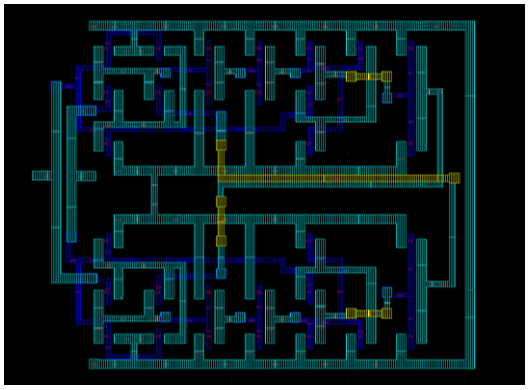

Fig.6 An Extracted View of Low Glitch Phase Detector

III. PERFORMANCE ANALYSIS

A. UP and Down Output Waveforms

The implemented phase detector circuit can be analyzed in two different ways. One way in which CLK_IN leads CLK_OUT, and the other in which CLK_IN leads CLK_OUT. The UP pulse is the difference between the phases of the two clock signals. This UP pulse indicates to the rest of the circuit that the feedback signal needs to speed-up or catch-up with the reference signal.

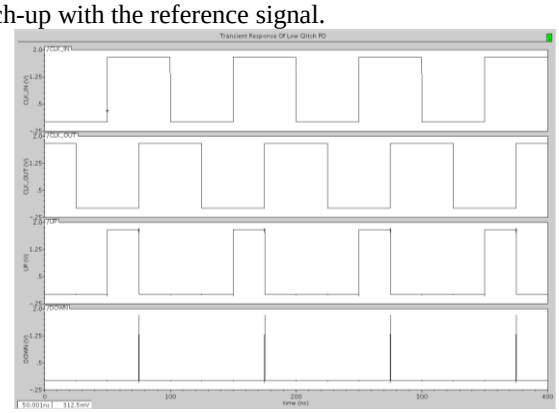

Fig.7 Low Glitch Dynamic PD Simulation I (CLK_IN leads CLK_OUT)

In the second case CLK_OUT is leading CLK_IN. In this DOWN pulse represents the difference between the phases of the two clock signals.

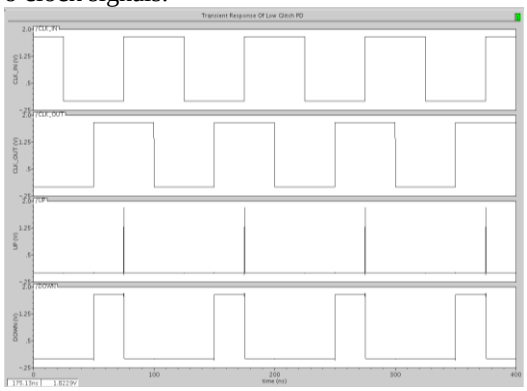

Fig.8 Low Glitch Dynamic PD Simulation II (CLK_OUT leads CLK_IN)

B. Glitch Comparison

The inputs to the PD are two signals which are having a period of 100 *ns* and with a phase difference of 90º (25 *ns*) in 180 *nm* technology with V_{DD} = 1.8*V*. On simulation, the flip-flop based PD has the duration of glitch as 590 *ps* [75.00 *ns* to 75.59 *ns*] which is quite high as compared to introduced low-glitch PD. The zoomed-view of glitch in flip-flop based PD is clearly shown in Fig. 9.

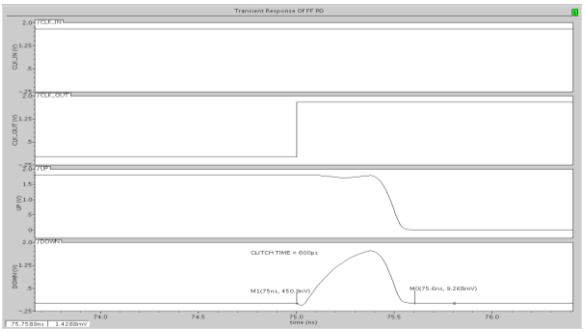

Fig. 9 Zoomed view of PD based on DFF [Glitch is from 75 *ns* to 75.59 *ns*].

The inputs to the low glitch PD are the same signals that applied to the prior circuit. The outputs of the two PD's are similar without zooming. The zoomed view establishes the advantage of the low glitch PD over the prior circuit. The glitch at the output of low glitch PD is much less as compared to PD based on flip-flops. The duration of glitch in the PD is 220 *ps* [75.00 *ns* to 75.22 *ns*] as shown in Fig. 10.

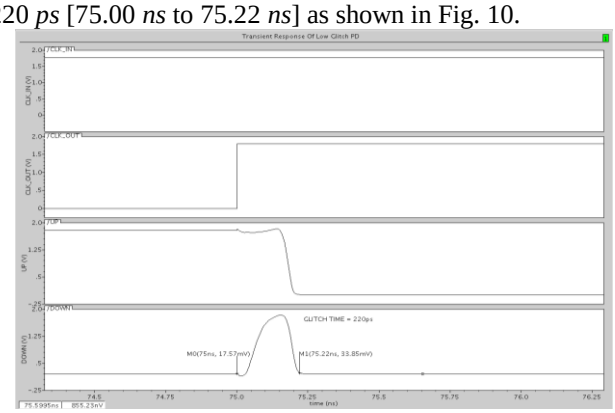

Fig. 10 Zoomed view of Low Glitch Dynamic PD [Glitch is from 75 *ns* to 75.22 *ns*].

C. Phase Noise

Phase noise simulation of Low Glitch PD is shown in Figure 11. CLK_IN and CLK_OUT are 50 MHz and have the same phase approximately. Phase noise computes the total noise contribution of the input signal to the circuit. Noise is contributed to PD from different sources such as dead zone and transistors. The phase noise of a DLL based system is affected by two main factors namely the phase noise of the input frequency by the crystal oscillator and the phase noise contribution by the delay chain. Low Glitch PD has phase noise of -156 dBc/Hz while flip-flop based PD has -156.3 dBc/Hz at 1 MHz offset as shown below in Fig. 11 and Fig. 12 respectively.

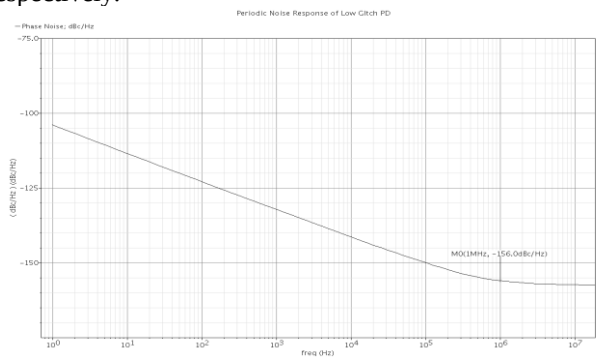

Fig. 11 Phase Noise of Low Glitch Dynamic PD

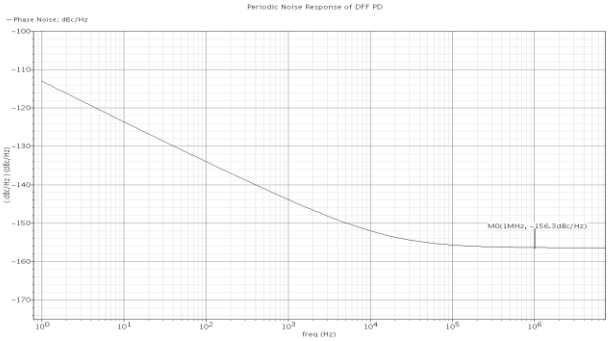

Fig. 12 Phase Noise of D Flip-Flop based PD

D. Phase Sensitivity

Sen*s*itivity of PD means the smallest difference the PD can detect and produce corresponding correct output signals, this leads to a conclusion that the higher the sensitivity, the better the PD. The low glitch PD is sensitive to even very small phase differences upto1 *ns* as shown below in Fig. 13.

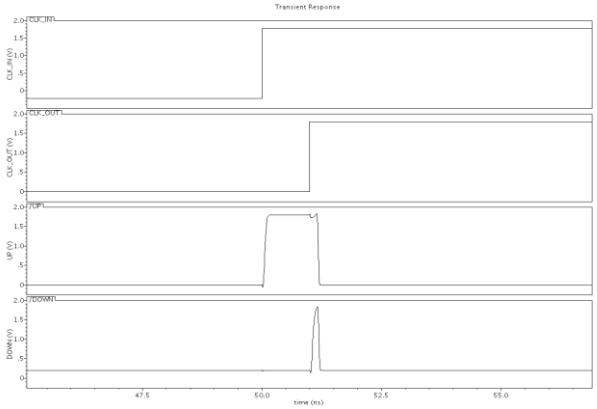

Fig. 13 Low Glitch Dynamic PD 1 *ns* Phase Difference

E. Comparison of DFF PD and Low Glitch Dynamic PD

Phase sensitivity, glitch time, and phase noise are the main characteristics of any PD. Table I represents different parameter analysis for the DFF based PD and Low Glitch Dynamic PD.

Table I: Comparison of Low Glitch PD and DFF PD

Parameters	D Flip-Flop based PD	Proposed Low Glitch Dynamic PD
Technology	180 *nm*	180 *nm*
V_{DD}	1.8 *V*	1.8 *V*
Phase Noise	-156.3 dBc/Hz	-156 dBc/Hz
Glitch Time	590 *ps*	220 *ps*
Glitch Period	75.00 *ns* to 75.59 *ns*	75.00 *ns* to 75.22 *ns*
Power Dissipation	221.686 μW	661.262 *pW*

IV. CONCLUSION

The proposed work presents two Phase Detector designs implemented in 180 *nm* CMOS technology. The glitch time, power dissipation and phase noise shows advantages of Low Glitch Dynamic PD compared to DFF based PD. The glitch time is 220 *ps* as compared to 590 *ps* of DFF based PD.

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Shirish Tripathi, was born in India in 1986. He received the bachelor's degree in Electronics & Communication Engineering at the Institute of Engineering & Technology, CSJM University, India in 2008. He did his post-graduation from Thapar University, India in VLSI Design & CAD in 2010. His thesis was focused on aligning the controlling clock signal for high-speed synchronous interface circuits by decreasing the static phase error. He served IBM India Private Limited from 2010 to 2012. From 2012 till date he is working as an Assistant Professor in Department of Electronics & Communication Engineering at PSIT, Kanpur, Uttar Pradesh, India.