Design and Synthesis of Reversible Fault Tolerant Carry Skip Adder/Subtractor

Prashanth. N. G, Manojkumar. S. B, Balaji. B. S, Naveena Pai G, Havyas. V. B

Abstract— Reversible logic will be having more demand in future computation technology because of its zero power dissipation under ideal conditions. This paper proposes the fault tolerant carry skip adder/subtractor by using parity preserving reversible logic gates. According to the control logic input the proposed design can works as a carry skip adder or carry skip subtractor.

Index Terms—Reversible Logic Gates, Parity Preserving reversible Logic Gates, Full Adder/Subtractor, Parallel Adder/Subtractor, Carry Skip Adder/Subtractor

I. INTRODUCTION

According to R Landauer [1] the traditional irreversible logic circuits i.e. made up by using conventional logic gates such as AND, OR, EX-OR etc. will generates a energy dissipation of kTln2 joules of energy for one bit of information to be lost during computation process. Where k is Boltzmann's constant = 1.38×10^{-23} J, T is absolute temperature at which computation process has been performed. The energy dissipation for one bit loss is a small value but this value can cause overheating in the circuit that will gradually decrease the life span of the circuit or device. C. H. Bennet [2] has shown that we can achieve zero power dissipation if the circuits are constructed using reversible logic gates. This paper proposes the design of fault tolerant carry skip adder/subtractor using parity preserving reversible logic gates. Fault tolerance is the property that will enables the system to continue its operation when the failure occurs in any one of the component. The faults or errors can also be find out by parity checking. In reversible logic fault tolerant circuits are constructed by using parity preserving reversible logic gates. A parity preserving reversible logic gate is the one in which input parity will matches with the output parity.

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II. REVERSIBLE LOGIC GATES

A reversible logic gate will be having equal number of inputs and equal numbers of outputs, and the inputs are easily retrievable from the outputs. A basic reversible gate will be having k inputs k outputs therefore it will be called as k*k gate. In reversible logic gates fan out are not more than one and also no feedback paths are allowed.

III. PARITY PRESERVING REVERSIBLE LOGIC GATES

A reversible gate is parity preserving gate when its input parity will matches with output parity i.e EX-OR of all input will matches with EX-OR of all output [3]. Parity preserving reversible logic gates are the basic building blocks fault tolerant reversible circuits. There are several parity preserving reversible logic gates has been proposed in the literature. Feynman double gate (F2G) [4], Ferdkin gate (FRG) [5], Islam gate (IG) [6], Modified Islam gate (MIG) [7] and New Fault Tolerant gates (NFT) [8] are few among them.

A. Feynman Double Gate (F2G)

It is a 3*3 gate with input vector I(A,B,C) and output vector O(P=A, Q=A ⊕ B, R=A ⊕ C). It will be having quantum cost of two. The Figure 1 shows the diagram of Feynman Double Gate.

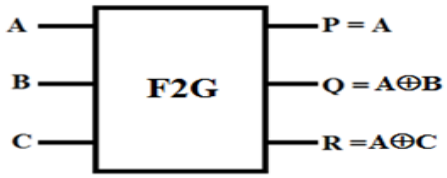

Figure 1 Feynman Double Gate (F2G)

B. Fredkin Gate (FRG)

It is a 3*3 gate with input vector I(A,B,C) and output vector O(P=A, Q=A′B ⊕ AC, R=A′C ⊕ AB). It will be having quantum cost of five. The Figure 2 shows the diagram of Fredkin Gate.

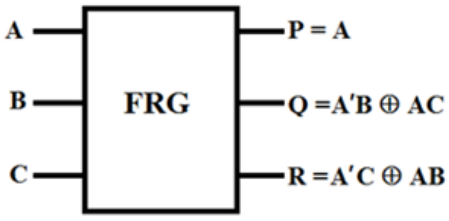

Figure 2 Fredkin Gate (FRG)

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C. *Modified Islam Gate (MIG)*

It is a 4*4 gate with input vector I(A,B,C,D) and output vector O(P=A, Q=A ⊕ B, R=AB ⊕ C, S= AB′ ⊕ D). It will be having quantum cost of seven. The Figure 3 shows the diagram of Fredkin Gate.

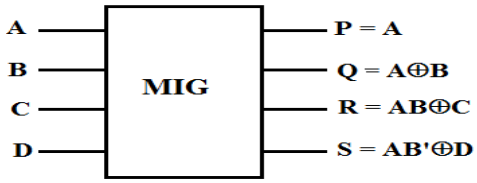

Figure 3 Modified Islam Gate (MIG)

IV. PROPOSED WORK

A. *Fault Tolerant Full Adder/Subtractor*

The Figure 4 shows the proposed fault tolerant full adder/subtractor. It can be designed using two MIG, two Feynman double gate and two Fredkin gate.

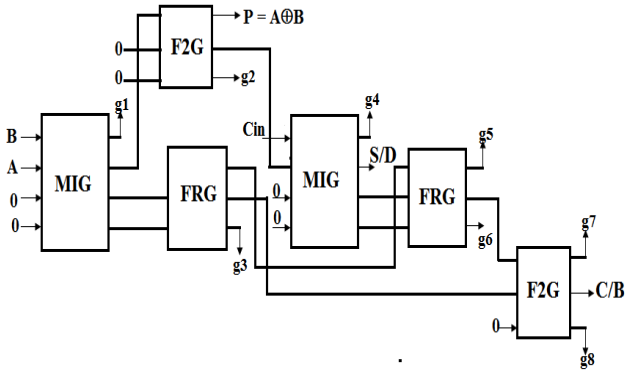

Figure 4 Proposed Fault Tolerant Full Adder/Subtractor (FT_FA/S_P)

B. *Fault Tolerant Parallel Adder/Subtractor*

The basic building block of parallel adder/subtractor is full adder/subtractor. The Figure 5 shows the proposed 4-bit Fault Tolerant Parallel adder/subtractor, it can constructed using 4 fault tolerant Full Adder/Subtractor with propagate (FT_FA/S_P). The proposed design will work singly a unit which consists of both parallel adder and parallel subtractor. The design will consists of control line ctrl which will selects adder or subtractor according the control logic input i.e. when ctrl is 0 it will acts as parallel adder and when ctrl is 1 it will acts as parallel subtractor [9].

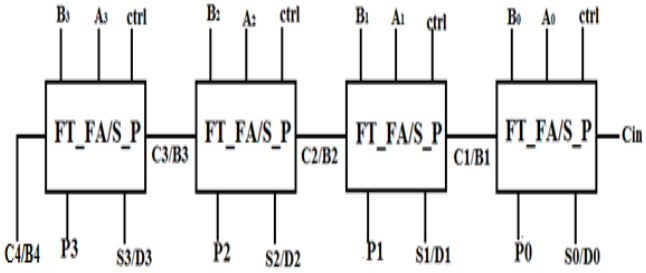

Figure 5 Proposed Fault Tolerant 4-Bit Parallel Adder/Subtractor

C. *Fault Tolerant Carry Skip Adder/Subtractor*

In the carry skip adder, delay is reduced due to the carry computation. In the full adder/subtractor operation, if either input is a logical one, the cell will propagate the carry/borrow input to its carry/borrow output. Hence, the nth full adder/subtractor carry/borrow input (C/B)n, will propagate to its carry/borrow output, (C/B)n+1, when P_n= A ⊕ B. In addition, the multiple full adders/subtractors, making a block can generate a "block" propagate signal P to detour the incoming carry/borrow around to the block's carry/borrow output signal. Figure 6 shows the proposed four bit fault tolerant carry skip adder/subtractor block. It is quickly determined by each block, that whether the block's carry/borrow input is propagated to its carry output. If the block propagate P is one, the block carry/borrow input Cin is propagated as the block carry/borrow output Cout [10].

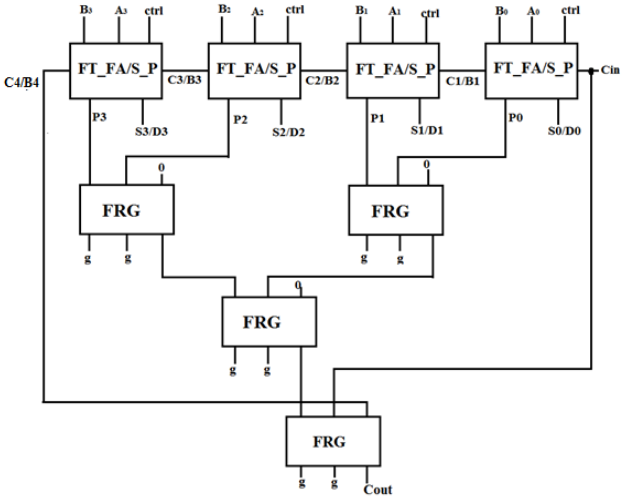

Figure 6 Proposed Fault Tolerant 4-Bit Carry Skip Adder/Subtractor

V. SIMULATION RESULTS

The entire architecture is modeled using Verilog language. The coding is done on Cadence Virtuoso tool and simulation is done on cadence SimVision tool. The Figure 7 and Figure 8 shows simulation results of proposed fault tolerant full adder and full subtractor, Figure 9 and Figure 10 shows simulation results of proposed fault tolerant 4-bit parallel adder and parallel subtractor and Figure 11 and Figure 12 shows simulation results of proposed fault tolerant 4-bit carry skip adder and carry skip subtractor respectively.

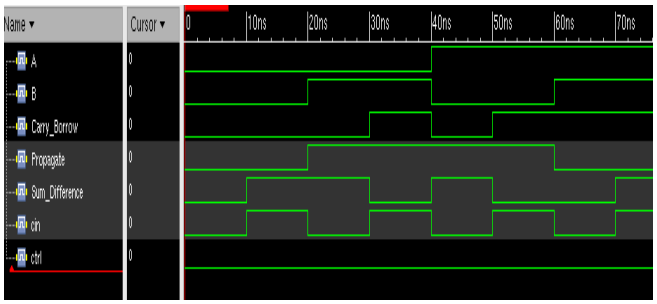

Figure 7 Simulation result of proposed fault tolerant full adder

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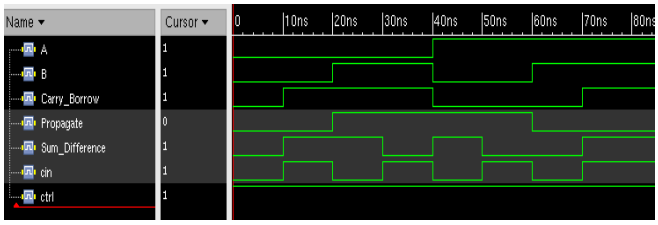

Figure 8 Simulation result of proposed fault tolerant full subtractor

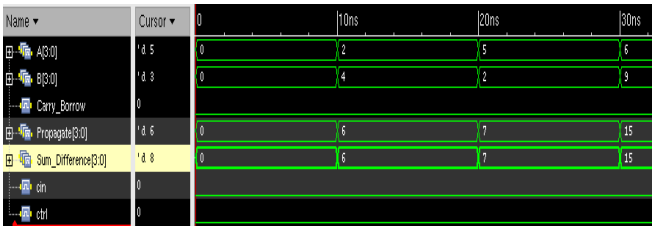

Figure 9 Simulation result of proposed fault tolerant 4-bit parallel adder

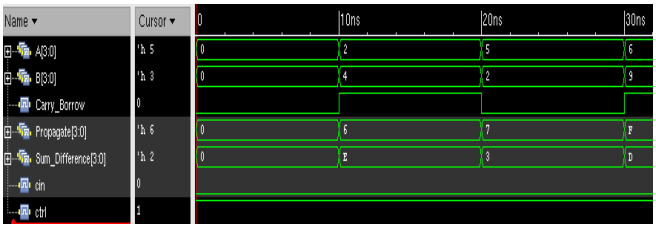

Figure 10 Simulation result of proposed fault tolerant 4-bit parallel subtractor

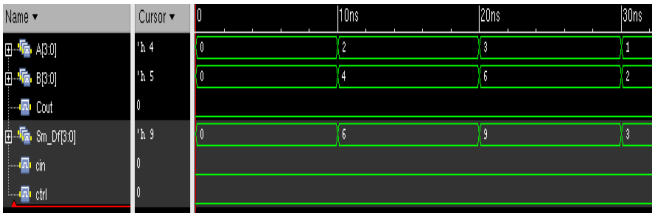

Figure 11 Simulation result of proposed fault tolerant 4-bit carry skip adder

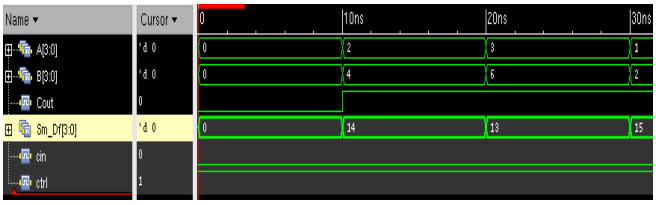

Figure 12 Simulation result of proposed fault tolerant 4-bit carry skip subtractor

Table 1, Table 2 and Table 3 shows the comparative results of different fault tolerant Full Adder/Subtractor, 4-Bit Parallel Adder/Subtractor and 4-Bit Carry Skip Adder/Subtractor

Table 1 Comparative Results of Different Fault Tolerant Full Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	9	9	10	30
Proposed Work	6	7	8	28

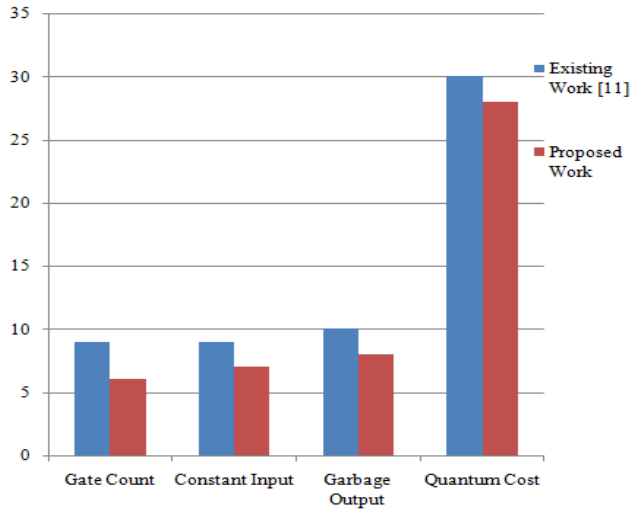

Figure 13 Graphical representation of comparison of different fault tolerant full adder/subtractor

Table 2 Comparative Results of Different Fault Tolerant 4-Bit Parallel Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	36	36	40	120
Proposed Work	24	28	32	112

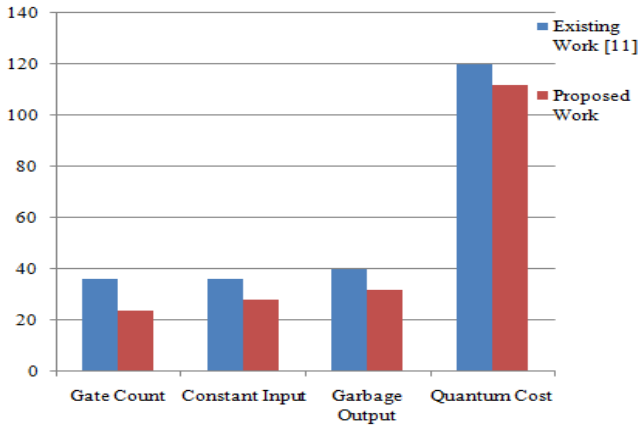

Figure 14 Graphical representation of comparison of different fault tolerant 4-bit parallel adder/subtractor

Table 3 Comparative Results of Different Fault Tolerant 4-Bit Carry Skip Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	40	39	48	140
Proposed Work	28	31	40	132

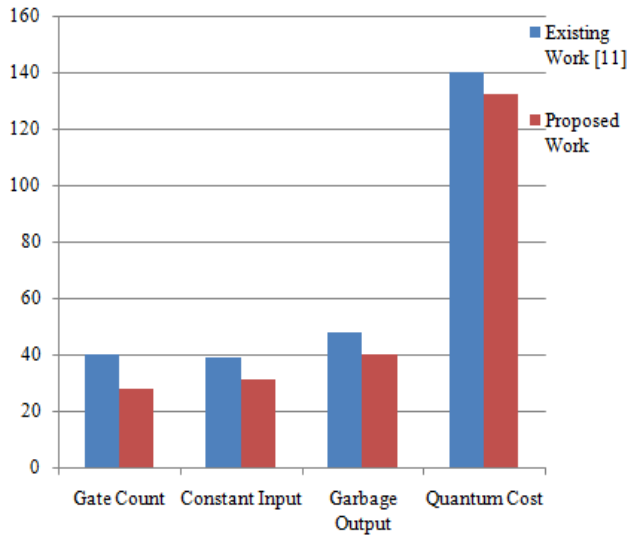

Figure 15 Graphical representation of comparison of different fault tolerant 4-bit carry skip adder/subtractor

VI. CONCLUSION AND FUTURE WORK

This paper presents efficient approach for the design of fault tolerant carry skip adder/subtractor. The proposed design can work as single unit that can acts as carry skip adder as well as carry skip subtractor depending upon our requirement. The proposed design offers less hardware complexity, less gate count, less garbage bits and constant inputs.

In future we are planning to design more optimized or efficient Fault tolerant carry skip adder/subtractor design i.e. less garbage bits and constant input, gate count and quantum cost.

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