Implementation of Power Management IC for Ultrabook Platform

Mairembam Birjit Singh, Vasudeva Banninthaya K, AtulSrivastava

Abstract:Power management is an important criterion in today's high efficiency mobile platform devices. As the technology of the mobile platform devicesadvances day by day, lots of techniques have been introduced for the efficient management of power on the mobile platform as well as to improve the battery life of the devices. This paper will present the implementation of the Power Management IC(PMIC) for power management on the Ultrabook platform and will feature the advantages of using PMIC for Ultrabook over the conventional Voltage Regulator Module (VRM) used for notebook like laptop. This paper will also highlight how the communication is done between the Embedded Controller (EC) and the PMIC in co-ordination with the multi-chip-package (MCP).

Keywords:Power Management Integrated Circuit (PMIC), Voltage Regulator Module (VRM), Voltage Regulator (VR), Embedded Controller (EC), Inter-Integrated Circuit (I2C).

I. INTRODUCTION

Today's portable batteryoperated devices are becoming smaller and slimmer and at the same time they should be able to operate for a long period of time. Along with the decrease in the size of these devices, the speed of these devices is also increasing day by day and the power consumption also increases. But at the same time, the battery technology developments are not improving by the same factor. As a consequence, intelligent power management becomes an important consideration to achieve the required battery life of the devices [1].Nowadays, lots of power management ICs are available in the market where the power management on the platform devices can be carried out efficiently.As today's computing world improves day by day, there is development in the design of new portable devices like tablets, smart phones, iPhones etc. and as for today's recent development in the field of portable computer is Ultrabook which is a subnotebook defined by Intel. Ultrabook has almost the features similar to laptop but due to the limited size, features like optical disk drives and Ethernet ports are removed. For the efficient operation and proper power management on the Ultrabook platform, this paper will present the implementation of Power Management IC and its advantage over the conventional VRM used for notebook like laptop.

II. OVERVIEW OF PMIC

The Power Management Integrated Circuit (PMIC) is an essential part of the Ultrabook Platform focused on high feature integration to minimize the system board area. It is the combination of different subsystems or features like voltage regulator, low voltage dropout linear regulator, LED driver, A/D converter,Clocks,Power MonitorUnit (PMU), Back up battery charger, Power source monitoring unit, Command and Control Unit (CCU). The PMIC device is controlled and programmed using I2C where PMIC will be acting as a slave and ECas the master. There is also a Serial Voltage ID (SVID) interface between the multi-chip-package (MCP) and PMIC for handling V1core voltage rail settings i.e. a voltage rail (a group of VRs) can be ON/OFF based on the SVID bits. The SVID logic will be there both on the V1 of the PMIC and the MCP to accomplish this task.The MCPis the combination of Central Processing Unit (CPU) and Platform Controller Hub (PCH).

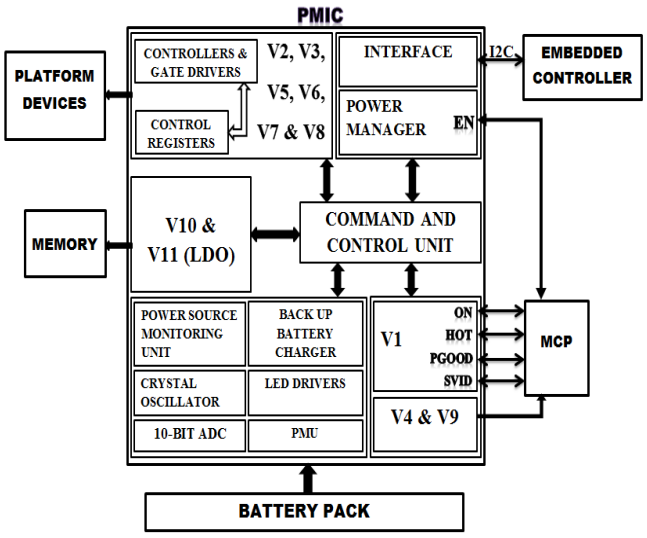

Fig.1: Interfacing of PMIC with platform devices, MCP and EC

The diagram showing the interfacing of PMIC with the platform devices, MCP and EC is shown in fig.1. From the diagram shown in fig.1, PMIC contains ten SMPS (V1 to V10) and one LDO regulator (V11). The VRs power the MCP, platform devices like camera, LCD panel, touchpad keyboard, DDR3, Bluetooth, USB ports, SSD, etc. and are critical to proper operation and functionality of Ultrabook platform based system. For the correct supply of power to different platform devices as well as to the MCP, there is communication between the MCP and the V1 via a number of bits called SVID. Initially, the PMIC voltage regulator V4 and V9 will supply a standard voltage to the SVID logic in the MCP. The MCP will then send the VID bits to the PMIC V1 regulator based on the load condition or the system states [2]. The different states of the system (S0, S3, S4 and S5) can be configured via the enable (EN) pin as shown in fig.1.

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Depending on the particular VID bits sent by the MCP, the EC will enable or disable a particular VR or group of VRs via VR Control Register using the I2C interface under the control and co-ordination of the Command and Control Unit (CCU).

The CCU is responsible for a number of functions like system reset control, interrupt management, routing data in and out of the PMIC configuration registers and SVID interface used by the MCP for control of the VR V1.

The Power Monitor Unit (PMU) shown in fig.1 is used to monitor the input power sources which may be AC (Adapter) or DC (Battery Pack) and also to monitor the output current/power and commands the platform to take action to reduce its power consumption if an overload condition occurs.There is also a circuitry in PMIC to generateclock signals by using two crystals oscillator which are required by the PCH, sensor hub and the EC. There should be proper hardware design so as to ensure that the clocks are enabled and disabled glitch-free. The Real Time Clock (RTC) data,status registers, oscillator, and timekeeping path of the RTC block are backed-up by a super capacitor or coin cell battery in case where main system battery is removed or deeply discharged. The 10-bit ADCis used for sampling battery current, AC adapter current, PMIC die temperature and system temperatures.PMIC requires four LED drivers for visual alert on system chassis.

III. PMIC I2C INTERFACE

The PMIC is controlled and programmed via EC by I2C interface. The I2C follows the standard Phillips I2C spec [3]. I2C is a 2-wire serial interface which consists of a data line (SDA) and a clock line (SCL) with pull-up structures. The embedded controller (EC) acting as a master controls the bus and is responsible for generating the clock signal and device addresses. The master will also generate specific conditions that indicate the START and STOP of data transfer.The PMIC works as a slave and supports the fast mode (400 kbps) of data transfer. The PMIC will receive and/or transmit data on the bus under control of the EC. The master i.e. EC initiates data transfer by generating a start condition which is the case when a high-to-low transition occurs on the SDA line while SCL is high as shown in Fig.2.

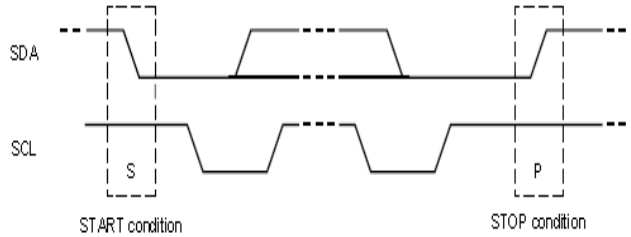

Fig. 2: START and STOP Conditions

All the I2C - compatible devices which are connected on the I2C bus must recognize the start condition. The master then generates the SCL pulses, and transmits the 7-bit address of the slave and the read/write direction bit R/W on the SDA line. All the I2C compatible devices should recognize the address sent by the master and compare it to their internal fixed addresses. The slave device with the matching addressshould generate an acknowledgementby pulling the SDA line low during the entire high period of the ninth SCL cycle as shown in fig.3.When this condition occurs, the master ensures that the communication link with the slave has been established and further communication with the slave can be processed. The master then generates further SCL signals to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). The transmission of 9-bit valid data sequence consisting of 8-bit data and 1-bit acknowledge continue as long as needed until the stop condition is generated by the master. The stop condition occurs when the SDA line is pulled from low to high while the SCL line is high as shown in Fig. 2. This will release the bus and stop the communication link between the master and the addressed slave.

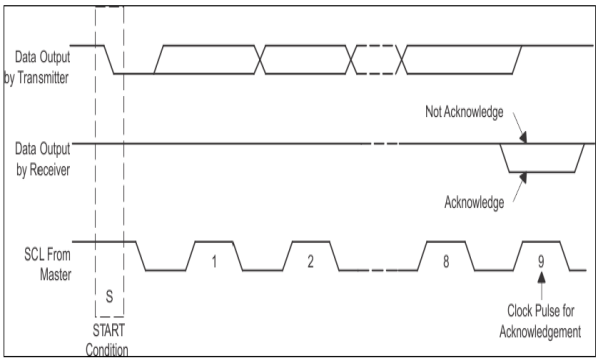

Fig.3: Acknowledge on the I2C –bus

IV. ADVANTAGE OF PMIC OVER CONVENTIONAL VRM

Almost all the desktops as well as the laptops use the conventional Voltage Regulator Module (VRM) to power the CPU, PCH and the platform devices for the proper operation and functionality of the desktop platform or the laptop platform. This Voltage Regulator Module (VRM) will have only the voltage regulators where the number of voltage regulators to be incorporated depends on the particular design. The control of these VRs is mostly based on the voltage mode Pulse Width Modulation (PWM) control method. As the VRs are operated in PWMmode, the efficiency of the VRM is compromised at the light load.

On the other hand, PMIC which will be used in Ultrabook platform employs the DCAP controlmethod where it allows the VRs to operate with Pulse frequency modulation (PFM) mode at light load and with PWM mode at heavy load [4].Pulse frequency modulation (PFM) also known as the power save mode [5] in Texas Instrument datasheet is a switching method used to improve the efficiency at light loads. As the VR operates with PFM at light load currents and PWM at heavier load currents, this allows the VR to maintain high efficiency over a wide range of output current or load current maintaining an efficiency of almost greater than 90% for a wide range of load. PMIC has also the ability to power the MCP and the platform devices during the connected standby (CS) mode [6] where a very low current will be required (in termsof mA) while maintaining the required regulated voltage level. This will help to improve the battery life of the overall system.The design of VRs of the PMIC employs a multi-output IC chip where a group of VRs are designed using a single IC chip. But in case of conventional VRM, each VR is designed using separate IC chip.

While the size of the conventional VRM and the PMIC remains almost the same, PMIC contains a number of other subcomponents like CCU, ADC,Clocks, Back up battery charger, LED driver and PMU in addition to VRs. This results in the reduction of nearly more than 25% in the size of the system board area as all the power related components which are to be there on the system board have been combined together in the PMIC itself.

V. EXPERIMENTAL OUTPUTS

The I2C read and write operation of the PMIC is shown in fig.4 and fig.5 with yellow colour channel as the SDA line and blue colour channel as the SCL line.

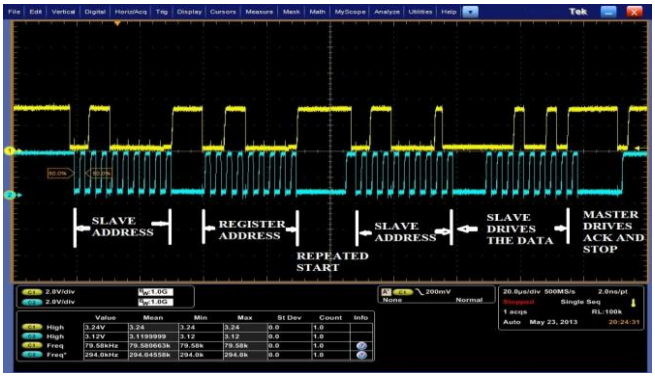

Fig.4: PMIC read operation

In the read operation, the master, EC transmits the 7-bit slave (PMIC) address whenthe start condition occurs and then R/W bit = 0 on the SDA line. Once the slave address is acknowledged, the master transmits the particular register address of the PMIC where the data has to be read. Upon acknowledgement of the register address, the master generates a repeated start condition and then transmits the slave address along with the R/W bit = 1 so as to receive the data from the slave. When the slave address is acknowledged, the slave transmits the data to the master. Now the master should acknowledge upon receiving the data and then stops the communication if the required data is read. In the write operation as shown in fig.5, the master transmits the slave address along with the R/W bit = 0 upon detecting the start condition. Once the address is matched, the slave should generate the acknowledgement. Then, the master transmits the register address of the PMIC where the data is to be written. When the master receives the acknowledge signal, it will write the data to the particular register and then generate the stop condition if the communication is accomplished.

Fig.5: PMIC write operation

The voltage regulators of the PMIC have the ability to operate in PFM mode during light-load condition and PWM mode during heavy loading condition so as to improve the overall efficiency of the system during the entire load condition. This can be accomplished by setting the particular bits of the VR control register by the EC. The transition between the PFM mode to PWM mode and vice versa is shown in fig.6 and fig.7 where yellow channel represents the switching signal and the blue channel represents the output voltage of the voltage regulator V4.

Fig.6: PFM to PWM transition of VR V4

Fig.7: PWM to PFM transition of VR V4

The soft start-up waveforms of the voltage regulator V4 at light load and full load is shown in fig.8 and fig.9 where yellow channel represents the output voltage of the VR V4 and the blue channel represents the switching signal. From the fig.8 and fig.9, it is observed that the device starts up smoothly under no load as well as for full load as there is no overshoot or voltage fluctuation observed in the output waveform of the VR V4.

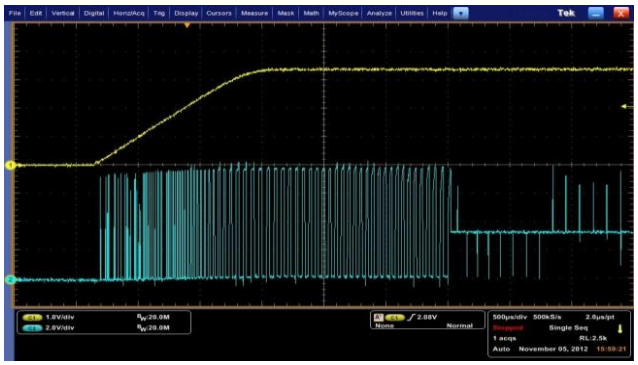

Fig.8: Start-up waveform at light load

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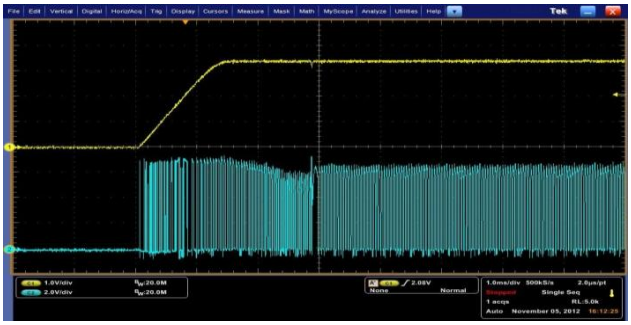

Fig.9: Start-up waveform at full load

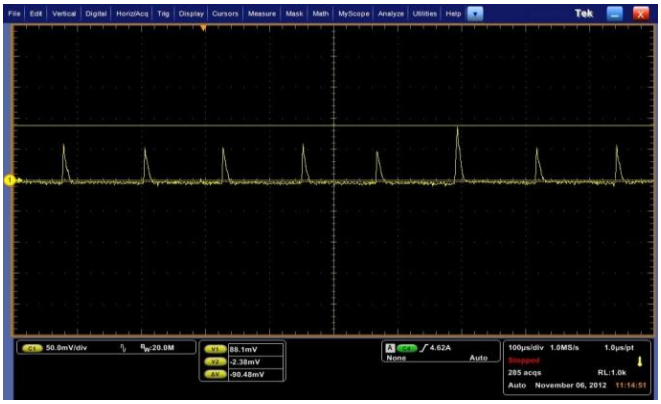

Fig.10: Output ripple at no load

The output ripple voltage at no load and full load is shown in fig.10 and fig.11. At no load, the output ripple is approximately around 90mV and at full load it is approximately around 45mV. Both the ripple voltages is well within the specified ripple voltage of 165mV for a 3.3V output (assuming ripple voltage = 5% of output voltage). This shows that the PMIC VRs are providing the regulated output voltages when the load changes from no load to full load.

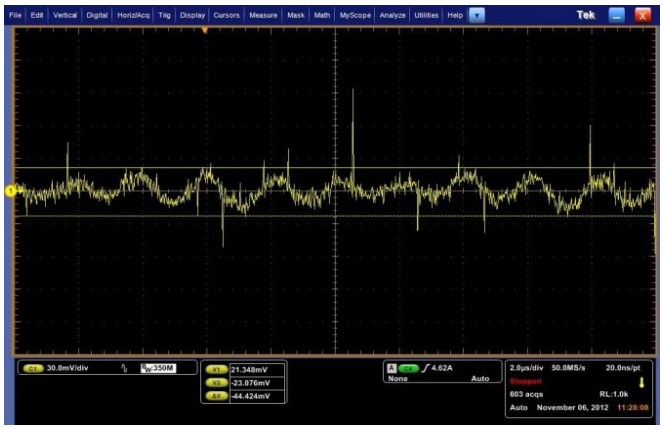

Fig.11: Output ripple at full load

VI. CONCLUSION

The implementation of the PMIC for power management on the Ultrabook platform is presented in this paper. The advantage of using the PMIC for Ultrabook application over the conventional VRM is also highlighted in this paper. As the size of the today's portable device reduces day by day, PMIC plays a very significant role in reducing the size of the Ultrabook platform. PMIC also helps in improving the efficiency of the system. It has the capability to supply the required regulated voltage with a very low current during the connected standby mode, thereby improving the battery life of the device. This paper also highlights how the voltage regulators of the PMIC can be controlledor programmed to achieve high efficiency during the different loading condition.

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