High Performance and Low-Power Full Adder

Mohammad Hassan Chamansara, Ayat Akbari, Hassan Taheri, Abdolhamid Sohrabi

Abstract*— Full adders (FAs) are essential for digital circuits including microprocessors, digital signal processors, and microcontrollers . Both the power consumption and the reliability of FAs are crucial as they directly affect: arithmetic logic units, floating-point units, as well as memory address calculations. This paper studies the effect threshold voltage (VTH) variations play on the reliability of a classical 28- transistor FA, and shows that reliability can be enhanced without increasing the occupied area, and while also reducing power consumption. An enabling transistor sizing scheme is used to improve on reliability without increasing power consumption (as reducing and limiting currents). The proposed FA in 16nm predictive technology model (PTM) is significantly more reliable (six orders of magnitude in case of Cout, and three orders of magnitude in case of Sum at 10% input variations) and dissipates 38× less than a classical FA, while being 6× slower.

***Index Terms*— Full adder, CMOS, power, energy, reliability.**

I. INTRODUCTION

Addition is the most common arithmetic operation used in a wide variety of digital applications. FAs are used in many arithmetic operations, and are crucial in arithmetic and floating-point units. They are also used extensively in cache and memory address calculations. The increasing demand for mobile electronic gadgets such as portable computers, cellular phones, and PDA‟s has raised the challenge for power-efficient circuits. Since FA cells usually lie in a critical path that determine the system overall performance, designing faster and low-power FAs was the driving force behind many results reported during the last decade [1]–[4]. The main objective of such designs has been to create faster FAs while also reducing their power consumption. For several decades increasing the performance by reducing the propagation delay was the main design objective of the VLSI community. During this time, the FA‟s performance and power consumption have also improved significantly due to the relentless scaling of CMOS devices. CMOS scaling was always used to implement faster, smaller and cheaper applications, which were optimized to work close to the minimum-delay operating point. However, with the massive scaling of the CMOS devices, both leakage and dynamic currents have been increasing exponentially.

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At the same time, with the explosion of battery-operated mobile applications (e.g., laptops, cell phones, etc.) during the last decade, energy efficiency became a stringent design objective, and is rapidly replacing the propagation delay as the main design objective.

Moreover, the scaling of the CMOS transistors deeper into the nanometer range introduces larger and larger parameter fluctuations/variations [5]–[7]. This leads to device-to device fluctuations in key parameters, including the threshold voltage (*V*TH), and drastically reduces the available reliability margins. However, most of the FA designs assumed that the circuits are implemented using reliable enough gates/devices. Therefore, reliability was not considered as one of the FAs‟ optimization criteria. It is only lately that the reliability of FAs has started to attract attention [8]–[12]. However, these papers have tried to evaluate and compare the reliability of exiting FAs without taking into account power and performance. In this paper a new transistor sizing scheme is used for improving the reliability of the classical 28-transistor CMOS FA (28T-FA) shown in Fig. 1. The proposed scheme *improves reliability (by reducing the effects of VTH variations), and reduces dynamic power (by reducing and limiting the switching currents)*. The paper is organized as follows. Section II explains the reversed-sized scheme, followed by reliability and power simulation results in Section III. Conclusion remarks are presented in Section IV.

II. THE EFFECTS OF VTH VARIATIONS

One of the fundamental limitations of the bulk MOSFETs is the accuracy of reproducing *V*TH over the large number of transistors in a chip. One major reason is the random. fluctuations of both *the number of dopants* and of *their physical locations*. Simulation results in [14] suggested that *V*TH variations could be approximated by a Gaussian distribution with standard deviation:

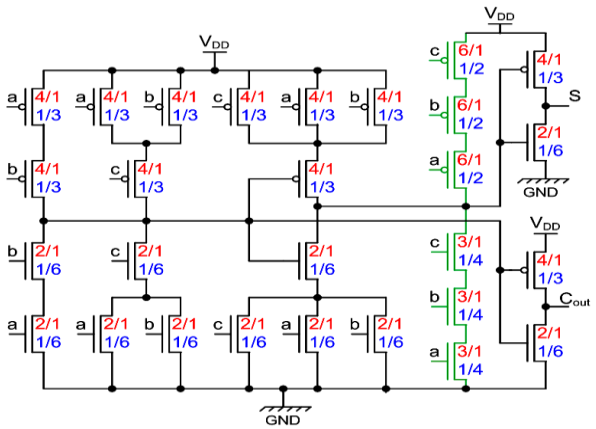

Fig. 1. 28T-FA: (a) Classical CMOS sizing as *W/L* (top, in red), and reveresed-sized as *W/L* (bottom, in blue).

$$\sigma \approx \frac{t_{ox} \times N_A^{0.4}}{\sqrt{L_{eff} \times W_{eff}}}, \quad (1)$$

where t_{ox} is the oxide thickness, *NA* is the channel doping, L_{eff} is the effective channel length (*Leff* = *L*×*a*), *W* is the effective channel width (*Weff* = *W*×*a*), and *a* is the technology size. It is clear from eq. (1) that σ is inversely proportional to *W* and *L*. Therefore increasing a transistor‟s area (by increasing *W* and/or *L*) will reduce σ, and consequently improves the transistor‟s switching reliability. In [15] we used σ to calculate the switching probability of failure of the nMOS and pMOS transistors. Fig. 2 shows the probability of failure (*PF*) of the nMOS (*PF*nMOS) and pMOS (*PF*pMOS) transistors when *L* = 1 and *W* = 2 in 16nm Predictive Technology Model (PTM v2.1, metal gate, high-*k*, and strained-Si) [19], [20], as a function of the input voltage variations. It shows that the probability of failure of the CMOS transistors depends on the transistor type (i.e., nMOS or pMOS), the applied logic at the gate terminal (i.e., logic high HI or low LO), as well as the input voltage variations (related to the noise margins). It also shows that *PF*nMOS is considerably higher than *PF*pMOS. Therefore, in order to improve the reliability of the 28T-FA one has to start by improving the reliability of the nMOS transistors first of all.

III. A NEW SIZING SCHEME

For classical CMOS, the maximum drive current when a transistor is switched “ON” is given by:

$$I_{ON} \propto \frac{W_{eff}}{L_{eff}} \times \mu^* \times C_{ox} \times (V_{DD} - V_{TH})^2, \quad (2)$$

where *Cox* is the oxide capacitance (per unit of area), and μ^* is the carrier effective mobility. The simplest and the most obvious way to reduce *I*ON (and the associate dynamic power) is to reduce *V*DD. As a result, low-power FA designs operating in sub-*V*TH have been proposed [2], [4]. However, operating in sub-*V*TH raises two major concerns. First, reducing *V*DD reduces *I*ON, which in turn degrades performance. Second, reducing *V*DD diminishes reliability [16]−[18] as amplifying the effects of *V*TH variations. To overcome the above disadvantages, a reverse-sized scheme [13] is used in this paper for improving both the reliability and the power consumption of the 28T-FA shown in Fig. 1. For several decades, maximizing performance has been the main objective for VLSI designers. Therefore, they routinely adjusted the sizing of the nMOS and the pMOS transistors not only to maintain the same *I*ON current when either the pull-up (*I*up) or the pull-down (*I*down) stacks are switched „ON“, but also for minimizing delays. One aim of transistor sizing is to balance the rise and fall times. In order to maximize performance while balancing the *I*up and *I*down currents, VLSI designers routinely set the length on the nMOS and pMOS transistors to minimum (*L*nMOS = *L*pMOS = *min*) to minimize resistance and gate‟s capacitance, and set *W*nMOS = 2×*L*nMOS. *W*pMOS was then adjusted (increased) based on the particular gate‟s topology such that *I*up = *I*down. This is needed in order to compensate for the difference in mobility between the holes (in case of the pMOS transistors) and the electrons (in case of the nMOS ones). As mentioned in Section II, increasing *W*pMOS does improve the reliability of the pMOS transistors. However, this does not affect he reliability of the 28T-FA as the pMOS transistors are lready more reliable than the nMOS ones (as shown in Fig. 2). Therefore, using this classical sizing scheme, improving the nMOS reliability by increasing *W*nMOS cannot be done without making *W*pMOS even larger. Such an approach would not only increase area but also power consumption, and clearly follows the widespread misconception that better reliability has to be traded off for larger areas and higher power consumptions. To overcome the constraints imposed by the classical CMOS sizing, we have proposed a reverse-sized scheme in [13]. The aim of the reverse-sized scheme is to improve he reliability of the nMOS transistors by making their areas larger than the areas of the corresponding pMOS transistors, while also reducing the dynamic power dissipation by reducing/limiting *I*ON. The reverse-sized scheme relies on the fact that changing the transistor‟s *W* and *L* dimensions does not only affect its reliability (see eq. (1)), but also the *I*ON current (see eq. (2)). Therefore, the reverse-sized method reduces *W*nMOS and *W*pMOS to minimum (*W*nMOS = *W*pMOS = *min*) in order to limit *I*ON. At the same time, it increases *L*nMOS to compensate for difference in mobility between the electrons and the holes. This is exactly the opposite of keeping *L*nMOS and *L*pMOS minimum and increasing *W*pMOS to compensate for the slower mobility of the holes.

A common objective of the classical and reverse-sized schemes is to balance the rise and fall times by properly sizing the transistors. This depends on the transistor type, and on how the transistors are connected together (i.e., gate‟s topology). Transistors connected in series should be sized differently than transistors connected in parallel. Fig. (1) shows the 28T-FA with classical sizing (in red) and reverse sized (in blue) for each transistor. It can be seen that for classical sizing the channel length for all the transistors was kept minimum (*L* = 1), while the channel width was set based on the transistor‟s type and its location in the circuit (the channel width being adjusted based on the number of transistors connected in series/parallel). Therefore, when two transistors are connected in series, the channel width is set to *W*nMOS = 2, while the channel width is increased to 3 when three transistors are connected in series. Additionally, to compensate for the slower mobility of the holes we have assumed that μ^*nMOS/μ^*pMOS = 2 (while exact values can be determined using Spice). Consequently, to match *I*up with *I*down the channel width of the pMOS transistors was adjusted such that *W*pMOS/*L*pMOS = 2×*W*nMOS/*L*nMOS. In case of the reverse-sized scheme, the design starts by setting the channel width for all the transistors to minimum (*W* = 1). The channel length of the pMOS transistors is then adjusted to maintain the same *I*up current (regardless of the number of transistors connected in series/parallel). Therefore, we set *L*pMOS = 3 when two transistors are connected in series, and *L*pMOS = 2 if three transistors are serially connected (see green transistors in Fig. 1). The channel length of the nMOS transistors is adjusted using the same approach for matching *I*up with *I*down (for the worst case combination).

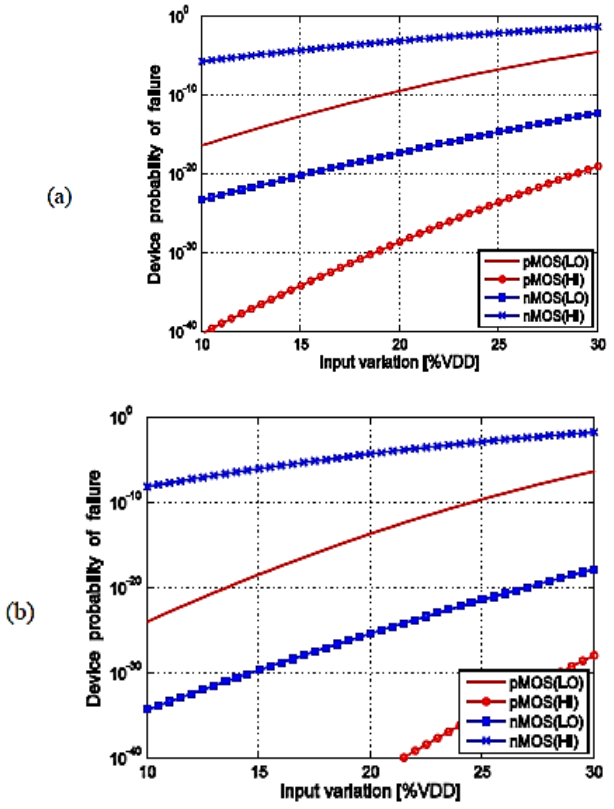

Fig. 3. Probability of failure of 16nm transistors in case of classical sizing: (a) nMOS = 2/1, pMOS = 4/1; (b) nMOS = 3/1, pMOS = 6/1.

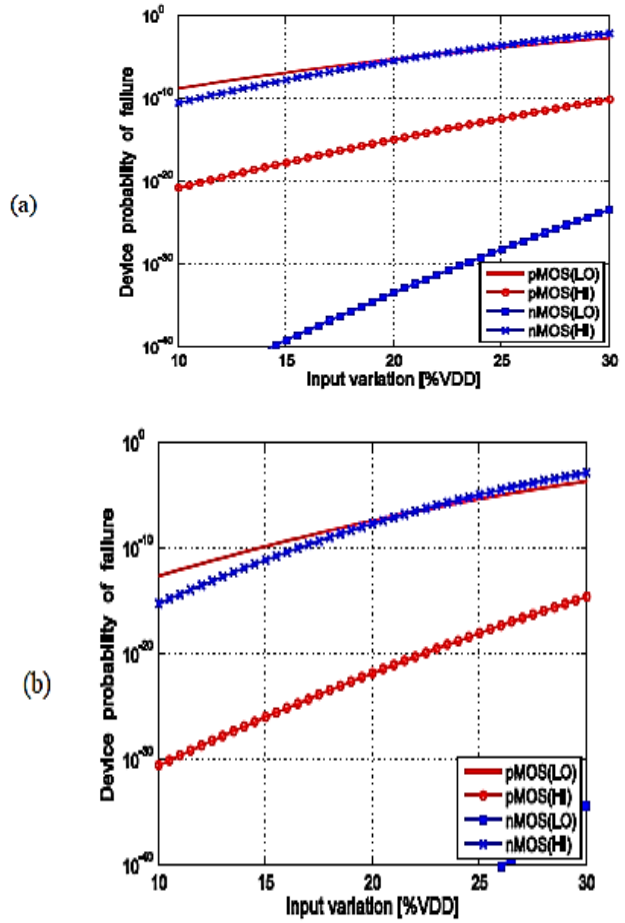

Fig. 4. Probability of failure of 16nm transistors when reverse-sized: (a) nMOS = 1/4, pMOS = 1/2; (b) nMOS = 1/6, pMOS = 1/3.

IV. SIMULATION RESULTS

Simulations were used to analyze and compare the reliability as well as the power consumption of the classical and the reverse-sized 28T-FA in 16nm PTM. GREDA (Gate Reliability EDA) tool [15], [21] was used to calculate the effect of *V*TH variations on the reliability of the 28T-FA starting from the reliability of the individual transistors. Fig. 2 shows that when the nMOS and pMOS transistors have the same area, *PF*pMOS is lower than *PF*nMOS. In case of classical sizing, Fig. 3 shows that increasing the channel width of the pMOS transistors to compensate for the slower mobility of the holes, increases the transistor area and reduces its probability of failure even lower (compare Fig. 2 with Fig. 3). On the other hand, when the reverse-sized scheme is used, increasing the channel length of the nMOS transistors increases their area, hence improves their probability of failure, which starts to match that of the pMOS transistors (as shown in Fig. 4). A second experiment compares the probability of failure of the classical and the reverse-sized 28T-FA (Fig. 1). Fig. 5 shows that using the reverse-sized scheme significantly reduces the *PF* of the 28T-FA. For example, at 10% input variations the *PF* of the *Sum* signal is reduced by 3 orders of magnitude (i.e., from 6.12E–06 in case of classical sizing to 6.17E–09 in case of reverse-sized). At the same time, the *PF* of the *C*out signal is reduced from 8.17E–06 to 2.33E–12, i.e., by more than six orders of magnitude. The last experiment reports power and delay when using the reverse-sized scheme, and compares these to those obtained by the classical CMOS sizing scheme. NG-Spice (ver. 22) was used to calculate the power, delay, and PDP for the two 28T-FAs. The simulations were done for 16nm PTM v2.1 at 27ºC and nominal *V*DD (700mV) ± 200mV (see Table I). It shows that the reverse-sized scheme at nominal *V*DD is able to reduce power consumption by 11.3×, while increasing delay by 8.7×. and reducing PDP by 30%. Using the reverse-sized 28T-FA at 900mV reduces both power and PDP by 38.8× and 6.3× respectively, while increasing the delay by 6.2×. The idea of iincreasing *V*DD goes against the normal trends, but is able to significantly improve on reliability as alleviates the effects of *V*TH variations (as presented in [12],).

TABLE I. POWER, DELAY, AND PDP MEASUREMENTS

	Classical			Reversed		
	500mV	700mV	900mV	500mV	700mV	900mV
Power	3.77E-08	1.53E-07	1.02E-06	5.83E-09	1.35E-08	2.63E-08
Delay	7.99E-11	3.11E-11	2.15E-11	1.43E-09	2.73E-10	1.34E-10
PDP	3.02E-18	4.75E-18	2.20E-17	8.35E-18	3.69E-18	3.52E-18

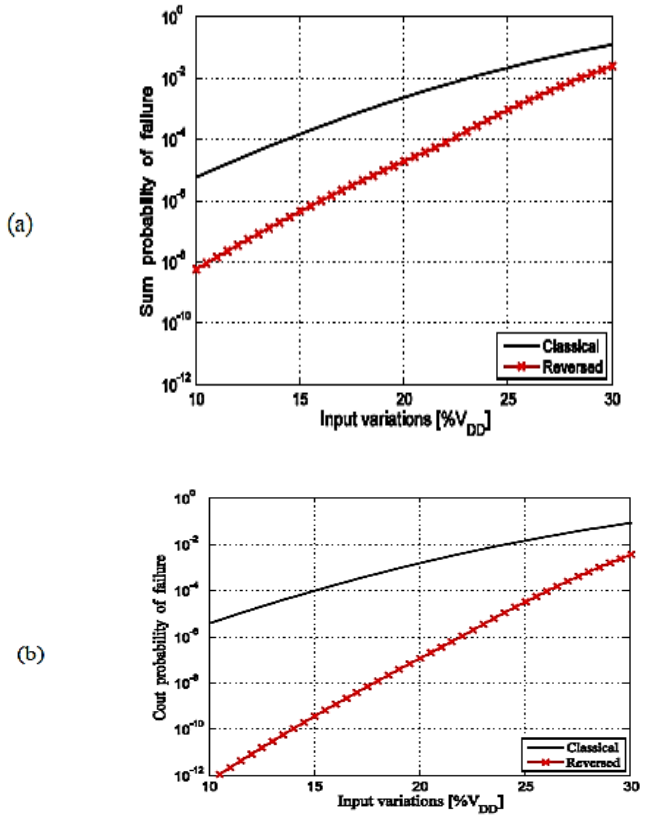

Fig. 5. Probability of failure for 16nm classical and reverse-sized 28T-FAs: (a) Sum signal; (b) Carry-out signal.

V.CONCLUSIONS

This paper has used a recently introduced reverse-sized scheme to improve on the reliability of the classical 28T-FA (by reducing the effects of VTH variations on the nMOS transistors), while simultaneously reducing both power and PDP (by reducing/limiting the switching currents). Simulation results confirm that the reverse-sized scheme can significantly improve the reliability of the 28T-FA (by orders of magnitude), while reducing both the power consumption and the PDP, maintaining roughly the same area, and only slightly degrading performances.

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