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Design Issues for Micro Electromechanical Systems (MEMS)

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Abstract—This paperdiscusses the design issue in the field of MicroElectromechanical System(MEMS).MEMS offer the handheld and consumer electronics industry great hope for enhanced functionality. MEMS based accelerometers, microphones, pressure sensors, antennas, RF switches and embedded memory chips are being integrated with IC products and leading to new applications. Definition of MEMS as the name suggests, it is the electronic with the mechanical parts(moving/non moving)on the same chip in the microscale. MEMS is the type of enabling technology in VLSI where the most important thing is the ability to add value to the existing or new systems/Ips in the field.Design process of any implication begins with the definition of the problem and the required problem specification followed by the generation of concepts ,the evaluation of concepts and then the product design.

Keywords- MEMS,VLSI.

I. INTRODUCTION

MEMS offer the handheld and consumer electronics industry great hope for enhanced functionality. MEMS based microphones, pressure sensors, antennas, RF switches and embedded memory chips, are being integrated with IC products and leading to new applications.

The Design process

Design process of any implication begins with *the definition of the problem* and the required *problem specifications* followed by the *generation of concepts, the evaluation of concepts* and then the *product design*. Since mems is technology emerged from VLSI many of the concepts are borrowed from the IC streams thus are similar in many aspects with other process design projects of integrated circuits. A unique aspect of mems is the that fabrication is expensive for one prototype testing before commercialisation of the product, as result a different approach is used in mems according to which to increase the number of iterations/fabrication it is more economical to design the test structure on a wafer itself. Below is ***the basic design process flow*** for commercialising the product. Here we can see that no of stages are visited more then once before the final product is put on the wafer in foundry,

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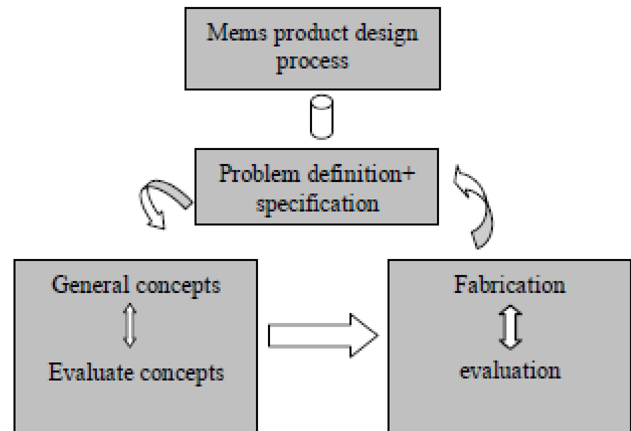


II. DESIGN TOOLS FOR MEMS

There are basically two models used to analyse the mems models namely- the physical and mathematical models, which can be in the form of closed form analytical models, or numerical model. The mathematical models that are available are the ***mat lab or simul ink***. Generally the numerical models are used for optimisation of the concept. At the system level lumped parameter modelling is usually required and thus the simul ink or spice or anysis packages are used.

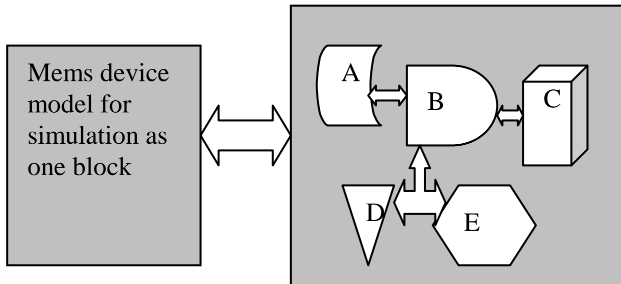
Unlike the IC CAD tools, *CAD tools for the mems are still in the phase of developing* and long way to attain matured phase because of the diversity in the mems concepts, devices, actuation methods and sensing mechanisms. ***The basic concepts exploited in mems are the electrostatic, induction, capacitor, thermo electromagnetic, optoelectronics, electro thermal, heat transfer, thermo resistive and many more yet to mentioned and to be discovered.*** Due to the variety of these concepts there is no single process or tool that can be used in the patent way to manufacture mems.

Finite element analysis

Mems device are constructed in three-dimensional geometries. The structural components of mems device can be subjected to thermal or mechanical loading during operation, which causes the thermal and mechanical stress to develop in the device and if it exceed the normal operating conditions can cause failures,

Mems structures can be multilayered as Ics consisting of dissimilar materials bonded together, where the materials are of different COEs, young's modulus and crystal structure. As a result the final element analysis is required foremost and proved to be the only solution to analyse the mechanical properties of mems structures. The basic principle of finite element analysis is that the whole model is divided into a finite number of smaller units called as element which are inter connected at corners or specific points called as nodes. Then complete analysis is

performed on the individual elements and combining the solution of the individual elements together generates the solution,
Below is the diagrammatical view as to what a finite elemental analysis is basically.



Below is the list of some commercialised mems devices, which are used widely in the auto and bio fields.

1. Inertial sensors – accelerometers/ gyroscopes
2. pressure sensors
3. micromotors
4. microbeams
5. Resonant beam deivces
6. Resonator comb drives
7. Light modulators
8. Micro tips
9. Micro grippers
10. Micro mirrors (presently the hottest field of development in mems)
11. Micro valves
12. micro pumps

Uptilt now we have covered the basic knowledge abt mems and the basic concepts used in the production of mems and what are the basic design and process tools used to make mems structure. In the later text we will cover some of the basic techniques used for micro fabrication, which are actually inherited by the IC industry, with some special processes generated for silicon micro machining. The basic material is the silicon along with some other material is also used in the production of specific mems structures.
Basically the si micromachining combines adding layers of materials over a silicon wafer with the process techniques like material deposition, patterning, etching etc. lithography plays the main role in mems in the delineation of precise pattern which is the main technique used in ic industry and is in the all time developing and matured technique as well.

Design Procedure

There is a basic step vise step procedure which is adopted to make mems structure after the project selection and finite elemental analysis and cad synthesis are completed to reach the final mems structure.

- Substrate selection
- Wafer pre cleaning for any oxides
- Formation of required oxides
- Spinning of adhesive
- Spinning of the photo resist
- Prebaking technique
- Masking of pattern using the uv light
- Exposure to light to remove any solvent & check photo resist uniformity
- Development of resist
- Post exposure & post baking technique
- Etching of the exposed oxide layers (si underneath as per design requirement)
- Stripping of the photo resist
- Packaging of the final mems structure

<u>Substrate selection</u>: -

This process includes selection of an orientation/plane specific si wafer for further processing depending on the mems structure to be designed, generally the commonly available wafers are <111,100,110 >plain wafers

<u>Wafer pre cleaning for any oxides</u>: -

Si gets oxidised slowly when kept in atmosphere forming a nano meter thick oxide layer on it, which is required to be removed before starting the process. The wafer cleaning technique is also done to remove any other solvent/oil/greasy materials present on the wafer that may get deposited while coming from the foundry to the laboratory. The common technique that is used is called as RCA cleaning process, which includes two steps called as RCA 1 & RCA 2.
In one step the oxides are removed and in the other step the remaining greasy/oily deposits are removed and the wafer is ready for further processing.

Oxide development/ thin film deposition on the wafer

There are a lot of ways in which a silicon wafer can be oxidised such as thermal oxidation, electrochemical iodization and plasma reactions; among these the thermal oxidation is the most commonly used technique. this technique helps in the generation of a stable & tenacious oxide layer on the top of si wafer, which is use d for a variety of process, features such as-
It acts, as a mask for etching process cause the rate of etching si dioxide is less as compared to pure silicon

- Diffusion of dopants at required depth in the si wafer
- Isolation layer & buried layer as an etch stop
- Sacrificial layer (surface micromachining)

To obtain a high quality silicon dioxide, it is done by oxidising si with either dry or wet oxygen at elevated temperatures (850-1200 degree c).
Dry oxygen :- si (solid)+ oxygen(gas)= silicon dioxide (solid)
Wet oxygen: - si (solid)+ water (gas) = silicon dioxide (solid) + hydrogen (gas)
Below is the figure of commonly used resistance-heated oxidation set-up

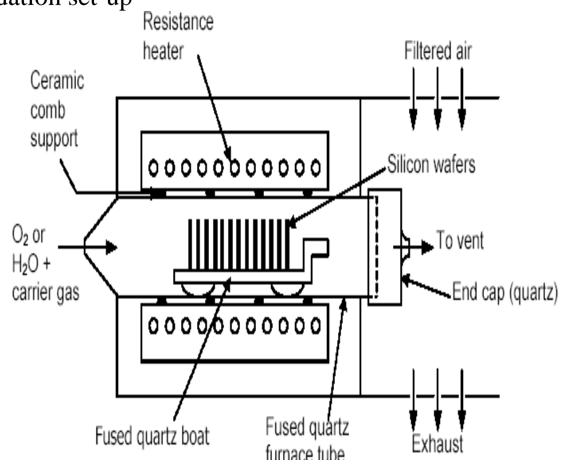


Figure of the setup used for thermal oxidation

Spinning of adhesive-

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The first step in the lithography process is that a thin layer of organic polymer is deposited on the wafer by spinning on it, the wafer is mounted on a vaccum chuck and a drop of the organic solvent is placed on it. This organic solvent is adhesive in nature thus it provides adhesion to the photo resist, which is deposited in the next step after this. The wafer is spined on a fixed rpm for some time such that the solvent gets deposited in a uniform way on the whole wafer. Generally adhesive that is used is HEXAMETHYL DI SILAZANE (HMDS)

Spinning of the photo resist-

Photo resist is a radiation sensitive/photochemical compound, which changes its properties when exposed to certain specific light radiations say UV or ire rays. Principally photo resist consists of

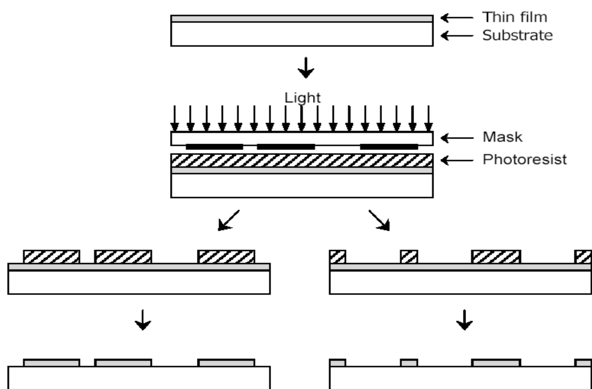
Polymer or base resin, which changes properties when exposed to radiations

Casting solvent- a liquid that is added to allow a free spin and formation of thin layer when the wafer and the photo resist are rotated together on a rotator same as used in spinning of adhesive.

Generally there are two kinds of photo resists namely-

- **Positive photo resist**- the photochemical reaction on application of the radiations weakens the polymer by rupture of scission of the side chain polymer as a result the exposed region becomes more soluble and easily removed in the development process of the photo resist.
- **Negative photo resist**- this photo resist is just opposite in its properties as compared to the positive photo resist. In this the compound becomes stronger by cross linking of the polymer's main chain as a result on development of this compound the regions unexposed to the light are easily removed as compared to the exposed region generally negative photo resist is commonly used.

THE BLOCK DIAGRAM BELOW SHOWS THE DIFFERENCE IN NEGATIVE AND POSITIVE PHOTO RESIST.

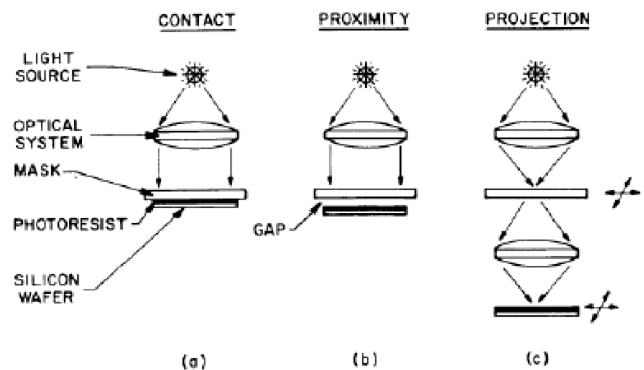


Prebaking technique-

After the application of photo resist and it's spinning to form the uniform layer, it still contains traces of approximately 15% of solvent that is added as a liquidifier to help in uniform layer of photo resist. It is necessary to remove it. This is done by pre baking technique, which is a process in which the wafer is heated to 75-90 degree C for 10 min to remove the solvent and stress to promote the adhesion of the resist layer to the wafer.

Masking of pattern –

Masking is done by using special mask, a stencil used t o generate a desired pattern in resist-coated wafers. It is nearly an optically flat glass transparent to UV light(350-500nm) or a quartz plate transparent to UV light ranging from 150-300nm. It contains chrome on one side, which is opaque to UV light and defines the pattern to be transferred. Throwing light on the mask aligned with the photo resist coated wafer by contact, proximity, and projection photolithography techniques do the pattern transfer. Depending on the kind of photo resist used the surface exposed (positive photo resist) gets weakened or the surface exposed (negative photo resist) gets strengthened.



Presently the projection photolithography is used mostly because since the mask doesn't come in direct contact with the wafer the mask can be used over a long duration of time.

Post exposure –

During the masking of the pattern as we see the surface is exposed to some kind of illuminations depending on the kind of applications. Post exposure is a process, which is sometimes desired as the reactions initiated during the exposure might not have run to completion. As a result to initiate new reactions or stop the reactions the wafer is again run into kind of post exposure treatments, which can be exposing to new type of radiations, treating with gases etc.

Development –

This process transforms the latent image into stable real image, which acts as a mask for further subtractive (etching) and additive (deposition) processes. During this process selective dissolving of the photo resist takes place. This is done generally by two techniques namely- wet development & dry development(still in explanatory stage)

wet development is done in two ways either by immersion development in which the wafers are cassette loaded and immersed in the bath of developer for limited time and agitated at specific temperatures resulting into dissolving of the photo resist(selectively). The second one is spray developer in which the wafers to be developed are sprayed with fresh solvents with a fan type sprayer.

Post baking technique-

During the development of the photo resist as described in the above step some of nearby resist is also affected because some of the developer penetrates inside the nearby resist layers, as a result of which the adhesion of the resist is weakened. This technique removes the remaining developing solvent from the wafer & strengthens the resist adhesion. This is similar to pre baking except that it takes place at higher temperatures of 120 degree C and for longer time of approximately 20 mins. It also improves the resist hardness

increasing the resistance of the resist to subsequent etching steps.

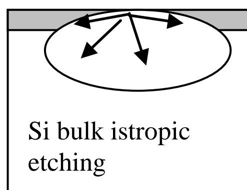
Etching (oxide layers/ si underneath as per design requirement)-

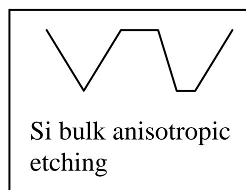
This process involves the removal of material by immersing the wafer in a liquid bath of the chemical etchant. This can be either done onto the si wafer itself or into a thin layer, which can be used as a mask layer for subsequent etches. There are two categories of etching si namely- isotropic etching or anisotropic etching.

- ***Isotropic*** etching attacks the material being etched at the same rate in all directions whereas
- ***Anisotropic*** attacks the material different in different directions thus giving more control over the shape required.

Wet etching is commonly used in bulk micromachining that is the bulk of the silicon is micro machined to form a structure. The diagram below shows the difference between the isotropic and anisotropic etching.

This form of etching is called bulk micro machining where the wafer is etched at a rate high rate as compared to surface micro machining where the wafer is deposited with number of layers of required metals/non-metals/polymers and then the selective etching is done to form the final mems structure not etching the main si wafer at all.





CHEMICAL VAPOUR DEPOSITION METHOD

This is the inherited process taken from IC industry for growth/deposition of various layers of metal or non-metals or polymers on the top of si wafer for mems structure development. This technique works at low/atmospheric/very low pressures. This is used to grow structural layers (poly silicon, silicon dioxide, silicon nitride), sacrificial layers like phospho silicate glass, and some metals like tungsten, aluminium, tantalum, copper etc. as a result we can say that this technique is very important and useful method for producing a diverse range of mems structures. A general procedure that is used to deposit any layer of deposit is that

First mixtures of process and carrier gases (inert) are introduced into the process chamber. The gas species move toward the surface of the wafer through both flow and diffusion. The reactants are then absorbed onto the surface and undergo chemical reactions on the surface. The by products that are gaseous in nature and continuously removed from the chamber. There are a lot of ways to provide energy required in the chamber either by thermal or plasma or latest the laser techniques.

As already mentioned above that there are many forms of cvd deposition process. These are

Atmospheric pressure cvd- as the name suggests in this form of cvd the pressure inside the chamber is atmospheric pressure & temperature ranges from 300-450 degree C. this is generally used for the epitaxial growth of si at very high rates of 150 nm/min approximately.

Very low temperature oxide cvd-

This cvd technique is widely used for growing si dioxide on the aluminium films by using si dioxide from silane and nitrogen reaction; at temperatures as low as 450 or even lower.

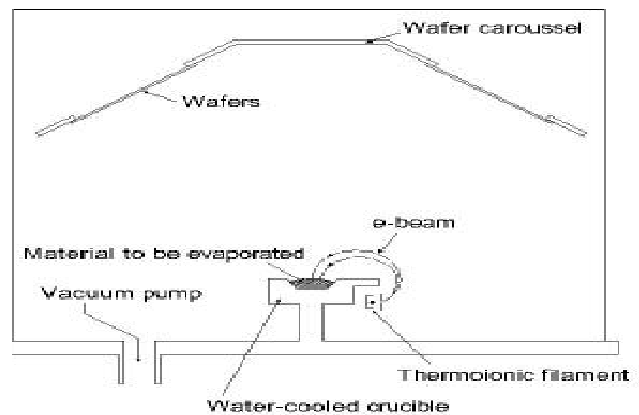
Low pressure cvd-

As the name suggests the operating pressure is as low as 10 pa thus allowing large no of wafers to be coated simultaneously without detrimental effects to film uniformity. The surface temperature control is the main aim in this type of cvd.

The crucible is used in all type of cvd techniques is similar to that used in the thermal oxidation accept that there is the temperature and pressure control mechanism inside. There are some more forms of cvd techniques available such as plasma enhanced chemical vapour deposition (pacvd), here the reaction is driven not with thermal energy but collisions with the energetic electrons in a glow discharge. The RF generator of a few 100 watts generates the plasma. This is generally used to deposit silicon nitride using silane and ammonia.

Up til now we have studied various aspects of the cvd technique there is other method of depositing layers, which does not rely on the chemical reactions.

Thermal vapour deposition. The common procedure is based on the condensation of a heated material in vapour phase onto a cold substrate in a vaccum. generally aluminium, gold, silver is the evaporated metals. There are different ways of heating up the metals to vapour phase which thus gives the classified name to that method. Some of the basic known methods are high current in a resistance (tungsten/neon lamp), electron beam, fro induction, laser beam. Below is the diagram of a basic setup, which is used to evaporate the material to be deposited on the wafer.



The above diagram is the basic set up for thermal evaporation of the host material to deposit it on the si wafer. As mentioned earlier depending on the heating medium the name of the setup changes, if we are using x-rays this is called as x ray evaporation, plasma enhanced thermal evaporation using rf generated plasma medium etc.

Si micro machining is divided into two branches as surface micromachining and bulk micromachining.

Surface micro machining

A process of combining structural materials and sacrificial layers for making mems structure on a si wafer, generally polysilicon is used as the structural material and silicon dioxide or related glasses (such as PSG) as the sacrificial material that is etched

afterwards in HF solutions as per design. This combination is the best-documented surface micromachining technique and it uses materials and etchants that are IC compatible. As we can see here the cantilever formed in this diagram is a released three dimensional area as a result of this utility surface micromachining plays a vital role in the telecommunication/optical field in generation free moving mirrors which are used as wave guides or signal directing mechanism.

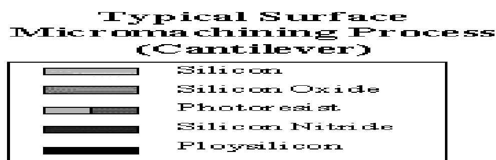
Fabrication issues

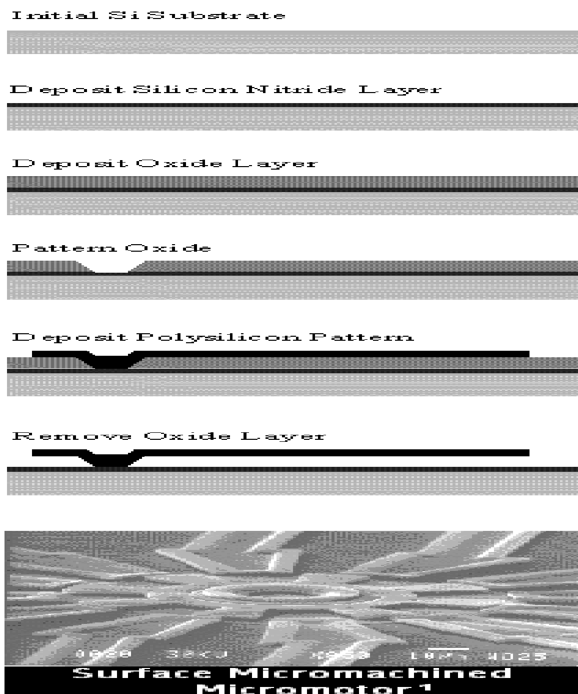
The basic fabrication steps of surface micromachining:

1) Deposition of the (silicon dioxide) sacrificial layer
2) Patterning of the sacrificial layer as mentioned above using masking & lithography.
3) Deposition of the (polysilicon) structural layer
4) Patterning of the structural layer as mentioned above using masking & lithography
5) Selective etching of the sacrificial layer in HF, rinsing and drying.

Bulk micro machining

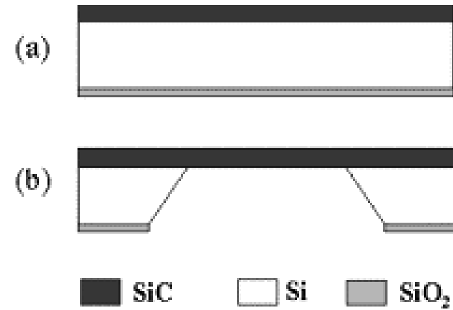
A process in which three-dimensional features are etched into the bulk of crystalline and non crystalline materials .as compared to surface micromachining, where features are built up, layer by layer, on the surface of a substrate (silicon wafer). Dry etching is used to define the surface features in the x-y plane (parallel to the wafer surface) and wet etching releases them from the plane by undercutting. In surface micromachining, the advantage is that shapes in the x-y plane are not restricted by the crystallography of the substrate. The biggest disadvantage is the restriction of microstructures to thin films.





The under cutting of the si plane is guided by using etch stops which are atoms of those metals or non-metals which are resistive to the particular etching solution as result restrict the further under cutting of the si wafer and giving the desired shape as per design. There are many methods used in this, the most common is the inherited ***boron etch stop***, which is commonly used in the IC industry.

Another common method used in the mems field is the ***electrochemical etch stop***. *The figure below clears the* difference in the bulk and surface micromachining. Here we can see the whole of the wafer has been etched away to get the desired structure where as in the surface micromachining only the structural and sacrificial layer are etched away and wafer remains almost untouched.



III. CONCLUSIONS

There are still many design challenges on the road for MEMS design. Some challenges are related to converting the existing expectations of MEMS designers to new modelling fields . Many still believe that for physical analysis and mechanical analysis in particular, finite elememnt simualtions are the only way. But in fact, over the last 10 years many alternate modelling levels and techniques have been made available that take into account more the work environment of the MEMS designers rather than just focusing on 3D solid model simulations other challenges that still exist are related to the manufacturing of MEMS, here the foundries can start to rely on design automation tools that can capture their process capabilities and process results for the MEMS engineer. Now also the packaging of MEMS can be included in the MEMS design process, this is possible for standard Packages and custom packages

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