Evaluation of Extension of Virtual Channel on Delay and Throughput in NOC

Mostafa Haghi, Elham Javadi, Hessam Khazraj

Abstract: - When designing a System-on-Chip (SOC) using a Network-on-Chip (NOC), delay and throughput are two critical factors to optimize. In fact to improve performance of the system designer should reduce the Delay cycles and raise the Throughput, but always there are some loss, to keep balance between these two elements designer has to adjust PIR in a certain range, to grant this, we need to know, for which purpose the system is going to be designed, it strictly depends on whether high Throughput or low Delay cycle is required. Extending the number of Virtual Channel (V.C) is a way to achieve this target. Here in this work we have selected three networks with in order 64,512 and 1024 IPs. The effect of V.C extension is evaluated on each one. We will observe, while varying the range of PIR , obtained results of simulator are different for V.C= 4,8,16, as we extend the V.C, delay cycle is reduced but in expense of more cost in some cases. In this paper we identify the take off points for Delay cycles and the points that has not be crossed by PIR rate level, to get a better trading off between effective elements of networks. Performance evaluation is conducted based on flit-accurate and open source System C simulator, BOOKSIM.

Keywords: NOC, SOC, PIR, VIRTUAL CHANNEL, DELAY CYCLE.

I. INTRODUCTION

As the size and complexity of integrated circuits (ICs) continue to grow, new design and implementation challenges arise. These circuits (chips) are even now highly complicated systems. Built of multiple subsystems and processors (cores) that are interconnected to form sub networks [1]. Depending on the architecture and tasks the system is conducting, large amount of data must be transferred among various processors (IPs) [2]. With current technologies this goal has to be carried out via wire based lines that is due to a deadneck in performance. While communicating between any two distant IPs in network that many intermediate Hubs are placed on the way, the amount of Delay cycles are raised up uncontrollable and from there performance of the system will be undesirable [3]. During recently years wireless technologies have an advantage of being a mature form of communication with many well-known applications implemented in wireless local area networks, cell phone and so on. This interesting knowledge in the wireless/radio frequency (RF) field will provide the integration of wireless interconnects for NOCs, or WINOCs [4]. Yet even with the relative great enhancement of wireless communication technologies, scaling this to very small sizes while concurrently scaling data rates to multiples of tens of Gb/s percents significant challenges in multiple areas, including network architecture, Wireless propagation modeling, antennas, low power circuits and device design [5]. It is expected that interconnection technology will become a restricted element in upcoming system-on-chip (SoC) designs [5]. A possible approach for coping with this issue is to apply an on-chip interconnection network instead of ad-hoc global wiring [6]. Such a network provides an on-chip communication infrastructure for interconnecting the system components. Many options for on-chip networks have been proposed [6][7][8][9]. While all of them are based on simple routers interconnected through network channels, (usually in a mesh topology), they differ in the techniques used for the router implementations. Among many solutions that alleviate effect of Delay in networks, extending the number of V.C is considerable. Wormhole routing with virtual channel flow control is a well-known technique from the zone of multiprocessor networks [6]. While area and power consumption are two major overheads [7][11], It allows minimization of the size of the router's buffers, while providing flexibility and good channel utilization. A general structure of a wormhole router with virtual channel flow control is depicted in *Fig. 2*. In this case the router has 5 input/output ports: 4 for connection with the routers those are next to, and one to link with the local node. At each input port the virtual channels (VCs), 4 in this example, are de multiplexed and buffering regulation is FIFOs. Status information is kept for every single bit of them. After the bits are out of port through FIFOs they are multiplexed again on a single channel which enters to a crossbar. The operation of the router is controlled by an arbitration unit (AU). It determines on a cycle-by-cycle basis, which virtual channels may advance sooner. Every V.C has the following states: *idle* – the VC is not used currently; *busy* – there is a packet using the VC; *empty* – busy VC with empty FIFO; *ready* – busy VC with nonempty FIFO. After initialization all VCs will be in the *idle* state. When a new packet arrives on a certain VC, the state of this VC is changed to *busy*. In order to start forwarding of the newly arrived packet the following information have to be provided for router: *output port (p)* – number of the output port the packet has to go *output VC (v)* – number of the VC of the *output port* the packet has to be sent on.

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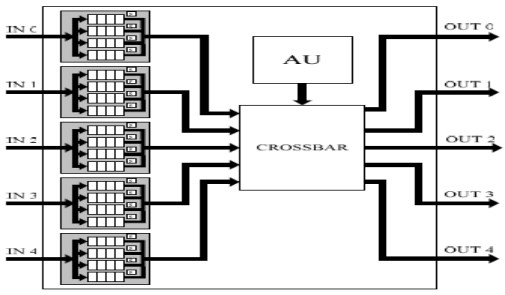

General Structure of a Virtual Channel Router with 5 Ports and 4 Virtual Channels

Changing the number of V.C is applicable to both Wire and Wireless interconnection networks, by applying this method, in fact we are dealing with architecture of router, some modifications have to be completed internally. By doing so, in following section we will observe how the delay is improved.

II. EXPERIMENTAL RESULTS

In this section we provide results of simulations for each case with different number of IPs (64, 512, 1024) and effect of virtual channel (V.C) on Delay and Throughput are evaluated under variation of PIR (0.01-1) in each state separately. This policy is started with 64 IPs in subsection 1 and ended up with comparing of all three cases of various numbers of IPs under different number of V.C in subsection 2.

Subsection 1

A) Evaluation of Delay and Throughput for: 64 IPs under 4,8,16 V.C.

In this case and all other states that will come in following subsection, we have ran simulator from PIR=0.01 up to 1, because for PIR below 0.01, the Throughput is very poor and in fact it's not economical, to designer wants to run the system under mentioned condition, that is the reason it is not taken into consideration. We want to prove that incrementing of number of V.C has a positive effect on reducing the Delay, on conditional and improve the performance. If we take a look carefully into figure.1 we observe, with increasing the number of V.C from 4 to 8 and then 16, under varying of PIR, the Delay is unchanged up to PIR=0.12 for all different number of V.Cs , when the PIR crosses the 0.12, two take off points (PIR=0.13, 4V.C=345 & 8V.C=358) are seen for V.C=4,8 at PIR=0.13 , in this status Delay is raised up uncontrollable because congested directions have occurred in network. In same network (64 IPs) under V.C=16 PIR still can be varied and Delay is under control and network runs well. In figure .1 one more point is observable that Delay is out of control and it occurs at PIR=0.14, it means that block direction happens for a network with 16 V.C in each port too, but where the capacity of router has been expanded from 8 to 16V.Cs, this phenomenon is showed up at higher level of PIR. To come a conclusion we must say if it's supposed to network runs under PIR below 0.12, the best decision that has to be taken is using V.C=4 for each port in router, because it costs less and the Delay will be the same as well as two other situations. Now in Figure .2 the effect of previous state is studied on Throughput. The results for Throughput are incredibly similar to each other for various number of V.C (4,8,16) in each PIR, while Throughput is expected to be improve with incrementing the number of V.C, but it doesn't, because wherein the number of IPs and V.Cs are not match for this network, that is the reason always some V.Cs are in idle state and are not useable due to not having a traffic between any two source and destination nodes in low rate of PIR, but for PIR above 0.13, when network is nearly getting congested, its anticipated that with having more number of V.Cs, it's possible to prevent a traffic or at least reducing it in network , from there all V.C are used and consequently Throughput gets improved.

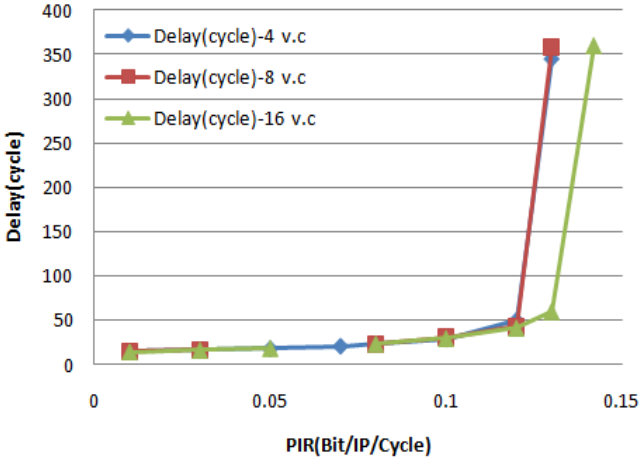

Fig. 1 Delay of Network with 64Ips Under Various no. of V.C.

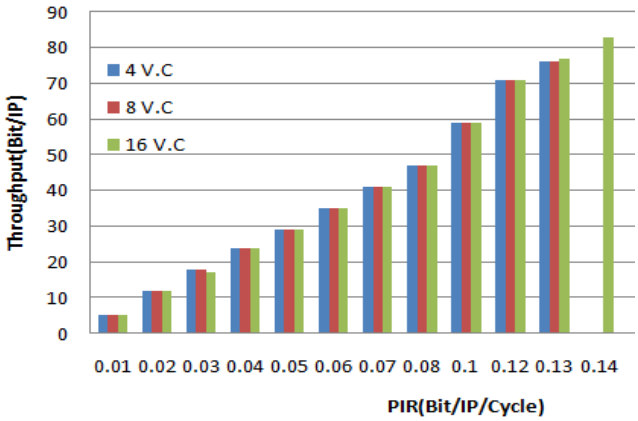

Fig. 2 Throughput of Network with 64 IPs under Various no. of V.C.

B) Evaluation of Delay and Throughput for: 512 IPs under 4,8,16 V.C.

In second case the number of IPs is increased by factor of 8, as the IPs are more than first case, therefore we expect an earlier traffic in directions, and the peak level of PIR becomes comes lower and consequently take off point will happen in lower PIR value. If the figure .3 is taken into consideration we will see that the mentioned expectation is match with obtained results of simulations. Let's observe fig.3 once again, the Delay value for all three kind V.C is the same, up to PIR=0.07, while for 64 IPs in previous section it was PIR=0.11, it occurs due to increasing the number of IPs and a heavy traffic in network. In spite of case a, in case b, when PIR crosses 0.07, this time graph shape of Delay for V.C= 8,

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undergoes a different direction in contrast with V.C= 4, it means that, with spreading of IPs in a network, with extending of the V.C, much more data can be placed in V.C's bit, therefore is helps to reduces Delay cycle. While PIR is rolling between 0.07 and 0.1, setting structure of router to V.C=8, is a wisely choice for network undoubtedly, because it has a same Throughput and Delay with V.C = 16, thus placing a 8 V.C in router, results in a less cost and complexity. Now with a glance into a Figure 4 we figure out that in range of 0.01≤PIR≤0.07, Delay and Throughput have the same value for diverse V.C = 4, 8, 16, then V.C= 4 is chosen, but with rising up of PIR rate (PIR≥0.1) equation is changed and this time V.C= 16 is suitable for two following reasons:

1. PIR is not supported by network when crosses 0.1, if V.C≤16, in this status Delay is not controllable,
2. Network has a greater Throughput for PIR≥0.1 and V.C = 16. In fact in this state, the number of IPs and V.C are match, and the network can obtain the best efficiency, all 16 V.C could be used appropriately.

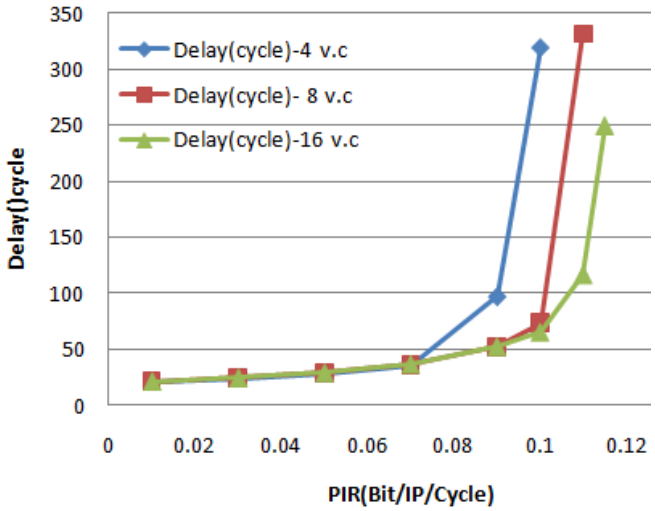

Fig. 3 Delay of Network with 512 IPs under Various no. of V.C.

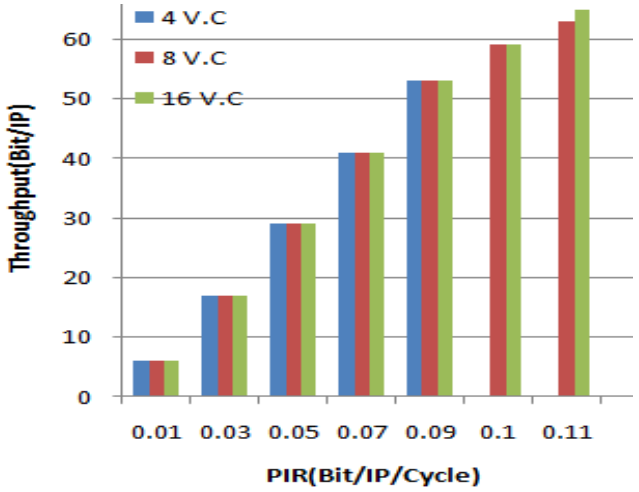

Fig. 4 Throughput of Network with 512 IPs under Various no. of V.C.

C) Evaluation of Delay and Throughput for: 1024 IPs under 4,8,16 V.C,

In the last case study, the network has been huger, now first we try to anticipate the behavior of the Delay and throughput and then will compare it with documentary results obtained from simulator. The logically policy is a earlier congested directions in network than other two cases a, reason is a greater number of IPs in network, as was mentioned before with communication between any two distant IPs, it's caused a more intermediate Hubs in directions and this increases the traffic in turn. Now we observe the behavior of each graph, it's seen obviously that our prediction was true absolutely. In case c the range of PIR that Delay is controllable within it, is restricted between 0.01 and 0.9 for all V.Cs. there is a tiny different between shape of graphs in case b and c for V.C = 4. In both cases the Delay cycle for all V.C is same, up to PIR= 0.07, but in spite of case b that take off point has very sharp slope, in case b, between controllable Delay point and take off point, one more point is observable, it shows that if the number of IPs are less, Delay cycles are manageable with less number of V.C. If the PIR crosses the PIR= 0.07 to get a better Delay cycle performance we have to switch the V.C to 8, but network can't be supported any longer when PIR≥0.08, because a heavy traffic occurs due to many numbers of intermediate Hubs and not enough available V.C to handle congestion via it, therefore network requires to switch to V.C = 16 for each router. The best range to get a high efficiency of V.C = 16 is 0.08≤PIR≤0.09, for PIR≥0.1 even 16 V.C doesn't support the network to work properly any longer, so it means with extending the number of IPs in network from one side and PIR rate from other hand, to manage the performance and Delay, the number of V.C has to be match with it. In Throughput case the results are almost same with two last cases, if the Throughput in a matter for user, he/she is allowed to design his network with 16V.C, if and only if the PIR≥0.08 otherwise it doesn't affect the efficiency of network and is waste.

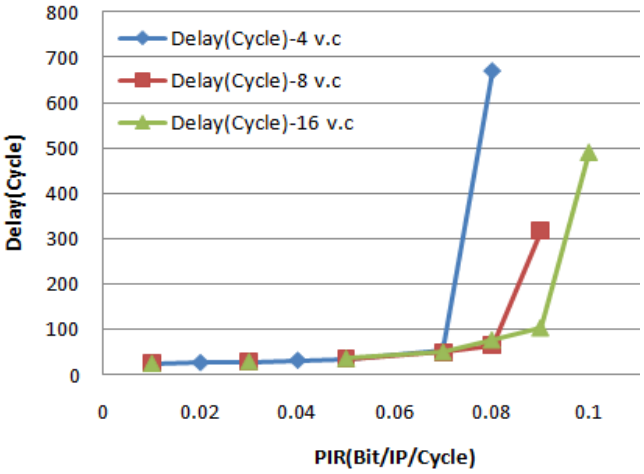

Fig. 5 Delay of Network with 1024 IPs under Various no. of V.C.

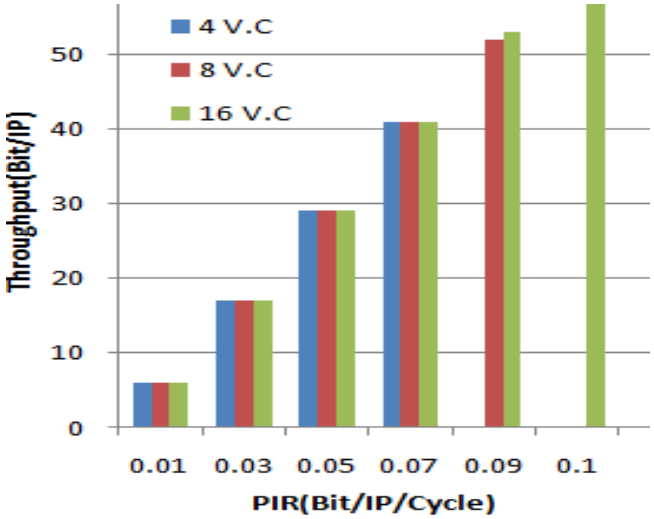

Fig. 6 Throughput of Network with 1024 IPs under Various no. of V.C

Subsection 2

In this part we are going to see how a hug network causes a congestion in directions and consequently heavy traffic, and ends up with an unreliable system if wouldn't be managed by different methods and solutions that are available for designer. Let's consider about three networks each content diverse numbers of nodes (64,512,1024),we want to see under same conditions how Delay parameter is going to varies for each one.

A) If we keep the number of V.C= 4 fixed for all networks, as we expect, the first network that reach to take off point is one with 1024 nodes, then 512 nodes and the last is 64 nodes, this was anticipatable, because many nodes are involved in network and directions are filled with bits carrying data between source and destination IPs, if designer wants to prevent this issue without any physical alteration or not to modify the design still he has a solution to alleviate this problem, designer has to keep the PIR less than 0.08, and to be in a safe margin less than 0.07 or else for holding performance and Delay acceptable, V.C has to be improved and this requires to a alteration in router design.

B) Number of V.C= 8, fixed for all networks. Here again the policy and solution are the same, the only different is higher level of PIR is achievable before take off point in Delay. Extending of V.C shows its positive effect obviously.

C) Number of V.C= 16, fixed for all networks. Results and analyze are similar. Remarkable statement to mention is range of PIR, that is extendable by incrementing the number of V.C, by changing the structure of router to provide this capability in it, in fact we create a potential of controlling the Delay and even reducing it, but while using this ability designer has to be careful that, achieving to a good Delay cycle may would be in expense of losing Throughput and much cost. While designing a network, it has to be mention by demander what is a major reason of the application. Low Delay cycle or Higher Throughput, then with regard to this matter, the direction and requirements are applied to achieve the best performance.

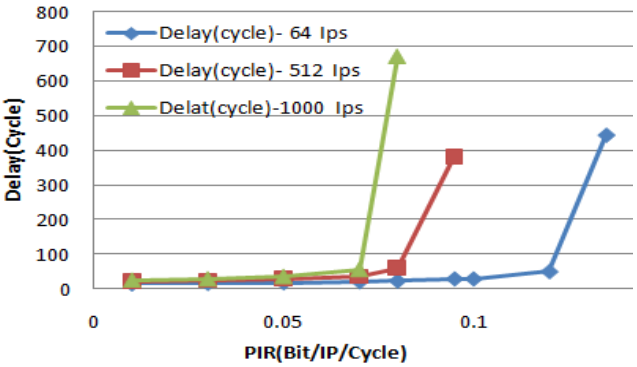

Fig. 7 Delay under 4 V.C.

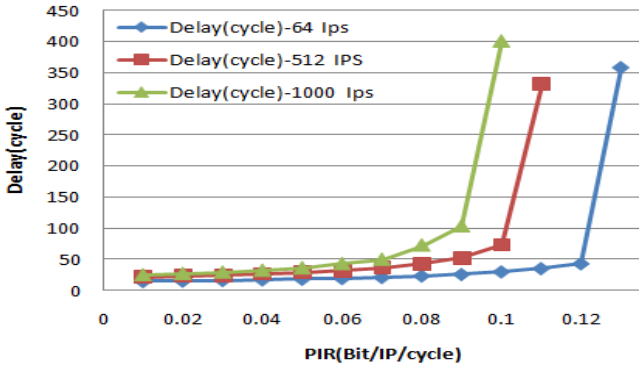

Fig. 8 Delay under 8V.C.

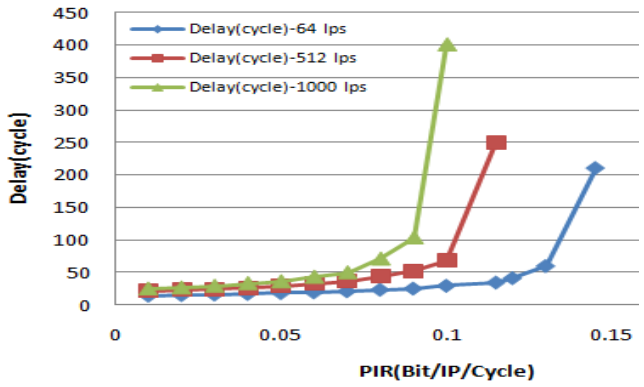

Fig. 9 Delay under 16V.C

III. CONCLUSION

Delay and Throughput are two critical factors that influence performance of interconnection in any network. Basically to get a better efficiency the application of the system has to be determined, means in trading off between Delay and Throughput which one should stay in heavy side in view point of user, one solution to improve the Throughput and reducing the Delay is extending the number of V.C. in this paper effect of various number of V.C on network with different number of IPs (64,512,1024) has been studied. As PIR is varying between 0.01 and 1, we figure out that for PIR≤0.07 for under all three cases Delay is controllable and there is no take off point before PIR=0.07, but value of Delay for diverse number of IPs is slightly different. Always two policies are observable: first: under equal number of IPs, the network with higher V.C has a lower Delay and in high PIR has a better Throughput (4<8<16), second: under same number of V.C, a network with lower number of IPs has a lower Delay cycle and reach take off point later. A remarkable point that should be

mentioned is always throughput for all states is the same for poor rate of PIR, it means that designer has to refuse using much number of V.C under low level of PIR. In the viewed paper we observed that using the most number of V.C is reasonable if and only if the maximum amount of possible PIR is applied.If we want to catch a high Throughput we need to use high rate of PIR.

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