A Survey of Multilevel Inverters

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Abstract - Multilevel inverter technology has become important over the years in the area of high power medium voltage energy control. This paper presents information about several multilevel inverter topologies, such as the Neutral-Point Clamped Inverter and the Cascaded Multicell Inverter. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulsewidth modulation, multilevel selective harmonic elimination and space vector modulation. Finally, developing areas such as electric vehicle propulsion converters and electric power grid system and other opportunities for future developments are addressed.

Index Terms - Multilevel inverter, topologies, modulation, comparison.

I. INTRODUCTION

In recent years, conventional two-level inverters, seen in Figure 1.1, are mostly used to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output voltages for the load, $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$ (when the inverter is fed with V_{dc}). To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 1.2. Though this method is effective it creates harmonic distortions in the output voltage, EMI and high $\frac{dv}{dt}$ (compared to multilevel inverters) [2]. This may not always be a problem but for some applications there may be a need for low distortion in the output voltage.

The concept of Multilevel Inverters (MLI) do not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 1.3, with lower $\frac{dv}{dt}$and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

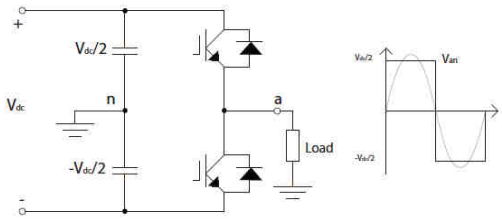

Figure 1.1: One phase leg of a two-level inverter and a two-level waveform without PWM

A three-level inverter design is similar to that of an conventional two-level inverter but there are twice as many valves in each phase-leg. In between the upper and lower two valves there are diodes, called clamping diodes [1], connected to the neutral midpoint in between two capacitors, marked n in the Figure 1.3. These capacitor build up the DC-bus, each capacitor is charged with the voltage $\frac{V_{dc}}{2}$. Together with another phase-leg an output line-to-line voltage with even more levels can be obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure 1.3, the result is a multilevel inverter with clamping diode topology.

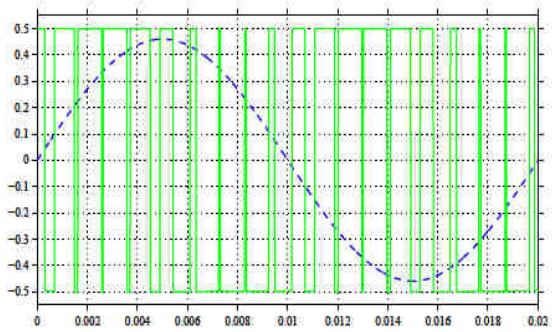

Figure 1.2: PWM voltage output, reference wave in dashed blue

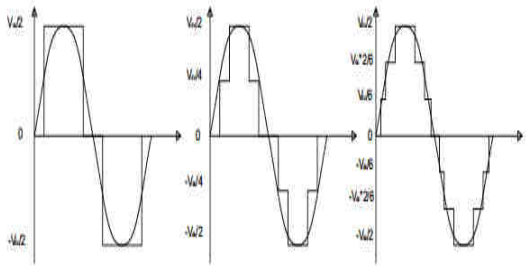

Figure 1.3: A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency

Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and $\frac{dv}{dt}$, generate smaller common-mode voltage and operate with lower switching frequency [2] compared to the more conventional two-level inverters. With a lower switching frequency the switching losses can be reduced and the lower $\frac{dv}{dt}$ comes from that the voltage steps are smaller, as can be seen in Figure 1.3 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, topologies with different properties have been developed, some of which will be discussed. The Multilevel inverter topologies that are investigated in this paper are: Neutral-Point Clamped Multilevel Inverter (NPCMLI),

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Capacitor Clamped Multilevel Inverter (CCMLI), Cascaded Multicell Inverter (CMCI), Generalized Multilevel Inverter (GMLI), Reversing Voltage Multilevel Inverter (RVMLI), Modular Multilevel Inverter (M2I) and Generalized Multilevel Current Source Inverter (GMCSI).

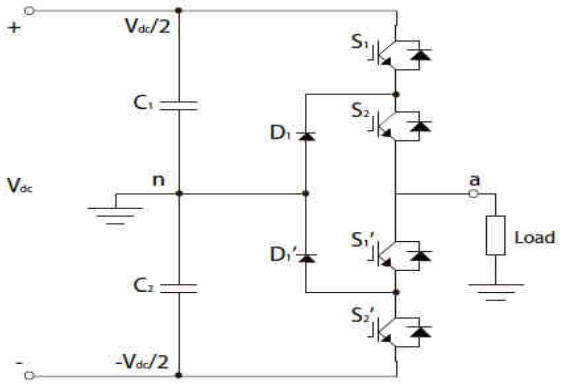

Figure 1.4: One phase leg of a three-level inverter

II. MULTILEVEL INVERTER TOPOLOGIES

A. Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI

According to patents the first multilevel inverter (MLI) was designed in 1975 and it was a cascade inverter (cascaded inverters will be presented in a later chapter) with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter, also called Neutral-Point Clamped Inverter (NPC) [2], see Figure 2.1.

In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by a even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line, see the left part of Figure 2.1. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an m-1 number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate).

In Figure 2.1 one phase-leg of a five-level NPC inverter is displayed. By adding two identical circuits the three phase-legs can together generate a three-phase signal where sharing of the DC-bus is possible. Take note that the required number of clamping diodes is quite high and for higher number of voltage levels the NPC topology will be impractical due to this fact [2]. The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. For example, in Figure 2.1 all diodes are rated for $\frac{V_{dc}}{4}$ ($\frac{V_{dc}}{m-1}$ in general) and the D_1' diodes need to block $3\frac{V_{dc}}{4}$ and therefore there are three diodes in series. However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. With this configuration five levels of voltage can be generated between point a and the neutral point n; $\frac{V_{dc}}{2}$, $\frac{V_{dc}}{4}$, 0, $-\frac{V_{dc}}{4}$ and $-\frac{V_{dc}}{2}$, depending on which switches that are switched on.

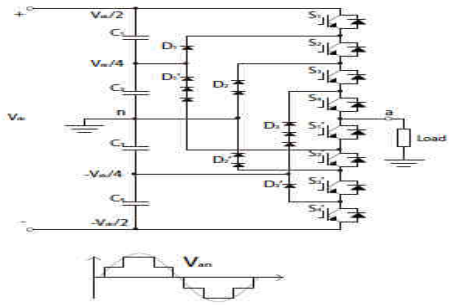

Figure 2.1: One phase-leg for a five-level NPC Inverter

To achieve the different voltage levels in the output a setup of switching state combinations are used. In Table 2.1 the different states for the five-level NPC inverter are shown. Note that there is the possibility to only turn on (and off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a fundamental switching frequency. From Table 2.1 it can be seen that for the voltage $\frac{V_{dc}}{2}$ all the upper switches are turned on, connecting point a to the $\frac{V_{dc}}{2}$ potential, see Figure 2.2. For the output voltage $\frac{V_{dc}}{4}$ switches S_2, S_3,S_4 and S_{01} are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and D_{01}. For voltage levels $-\frac{V_{dc}}{4}$ or $-\frac{V_{dc}}{2}$ clamping diodes D_2 and D_{02} or D_3 and D_{03} hold the voltage, respectively. For the voltages $\pm\frac{V_{dc}}{2}$ the current, when both voltage and current are positive (positive current goes out from the inverter), goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the D_x diodes and negative current through the D_x' diodes and also through the switches in between the clamping diodes and the load. For example, for state $\frac{V_{dc}}{4}$ positive current goes through diode D_1 and switches S_2, S_3 and S_4. In Figure 2.2 the turned on switches for every state are shown, switches in parallel to the thick dashed lines are on. In the figure the current paths are also shown, thin dashed lines, for every state and for both positive and negative current. For example for the $\frac{V_{dc}}{4}$ state the switches (positive current) or the diodes (negative current) are conducting and for the $\frac{V_{dc}}{4}$ state the current goes either through D_1 and three switches (positive current) or D_1' and through one switch (negative current). If there is a DC-source charging the DC-bus there is also currents flowing through the DC-bus to keep the DC-bus voltage constant. Table 2.1 also shows that some switches are on more frequently than others, mainly S_4 and S_1', as long as a sinusoidal output wave that requires the use of all voltage levels is created. When the inverter is transferring active power this leads to unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads and that current is drawn from nodes between capacitors. The total DC-bus voltage will be the same but the capacitors voltage will deviate from each other. While transferring real power current is drawn from, for example, capacitor C1 and C2 during different amount of time, as can be seen in the left part of Figure 2.3. The time intervals in the figure represent the discharge time and as can be seen C2 is discharged more, leading to unequal capacitor voltages. Also, during for example $\frac{V_{dc}}{2}$ the state current discharges both C1 and C2 but in the $\frac{V_{dc}}{4}$ state current is drawn from the point between C1

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and C2, discharging C2 but charging C1. This makes the voltages over the capacitors to deviate in a special way. When only transferring reactive power however the NPCMLI does not have this voltage unbalancing problem [3], see right part of Figure 2.3. This is because of that time intervals during which the capacitors charged and discharged are equal during reactive power transfer, as the figure suggests. To solve the voltage balancing problem an additional balancing circuit can be added or more complex control methods can be implemented. Due to the complications of the capacitor voltage balance, the NPCMLI at higher number of voltage levels is unusual.

Table 2.1: Switching states of one five-level phase leg. A "1" means turned on and "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	1	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

When it comes to component quantities, such as number of needed components and their ratings, some things have to be considered that have been partially mentioned in the text above. As mentioned the inner switches are on more frequently than the outer switches since they are used in several of the switching states. Because of this a different amount of RMS current will flow through the switches depending on their position, with higher current rating needed for the inner switches [3]. The position of the clamping diodes are also important to their ratings since they need to block different levels of reverse voltage depending on where they are connected. If equal ratings are assumed for every individual diode, for every extra level of voltage that needs to be blocked and extra diode is required. This in turn explains why the NPC topology is unpractical with higher amounts of voltage levels since, because of the extra blocking diodes, the number of diodes grows quadratically with the level m following the equation (m-1) * (m-2) [3]. This is however not valid for low voltage inverters, but since this paper focuses on high and medium voltage application this is still the case. As for the other components m-1 DC-capacitors, 2(m-1) main diodes and 2(m-1) switches are needed for the NPCMLI topology. For three-phase inverter of the NPC type the DC-bus can be shared and only the mentioned m-1 DC-capacitors are needed but the requirements for all other components are multiplied by three.

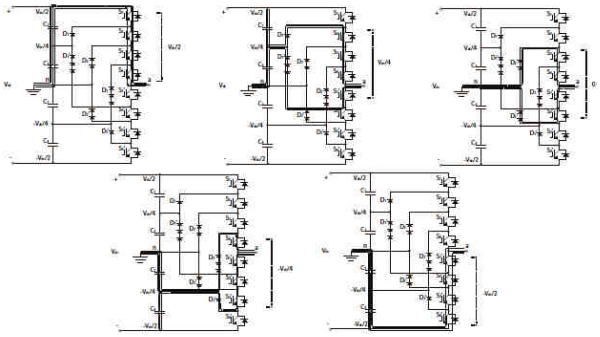

Figure 2.2: The thick dashed bar shows which switches that are on for every state. When both current and voltage is positive the current goes through these switches, otherwise through the diodes in parallel (depending on angle). Thin dashed line represent current path.

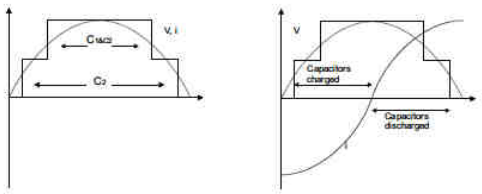

Figure 2.3: When voltage and current are in phase, to the left, capacitors are discharged unequally, but when the voltage and the current are 90 degrees out of phase, to the right, the charges is balanced.

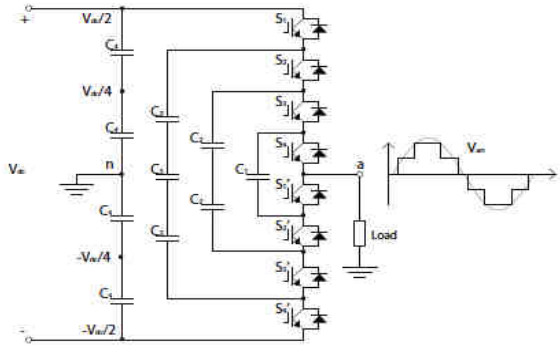

Figure 2.4: A Capacitor Clamped Multilevel Inverter with five voltage levels

B. Multilevel Capacitor Clamped/Flying Capacitor Inverter, CCMLI

A similar topology to the NPCMLI topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, which can be seen in Figure 2.4. Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. As for the NPCMLI, m-1 number of capacitors on a shared DC-bus, where m is the level number of the inverter, and 2(m-1) switch-diode valve pairs are used. However, for the CCMLI, instead of clamping diodes, one or more (depending on position and level of the inverter) capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position on each side of the a midpoint between the valves [3], see capacitors C1, C2 and C3 in Figure 2.4.

As can be noticed in Figure 2.4 the same number of main switches, main diodes and DC-bus capacitors as in the NPCMLI are used for the CCMLI. The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages the number of switching combinations increases [3]. Several switching states will be able to generate the same voltage level, giving the topology redundant switching states. The sum of a certain output voltage is generated by the DC-bus voltage $\pm\frac{V_{dc}}{2}$ and one or more of the clamping capacitors voltages added together. Since every capacitor is rated for the voltage $\frac{V_{dc}}{4}$ (in this five-level case, $\frac{V_{dc}}{m-1}$ in general), DC-capacitor and clamping capacitor alike, the output voltage, for this example $\frac{V_{dc}}{4}$, is generated by the DC-bus positive top value ($\frac{V_{dc}}{2}$) and

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the reverse voltage of clamping capacitor C1. The other voltage states work in similar ways but with the help of other clamping capacitors.

Table 2.2 shows some switching states for a five-level CCMLI and Figure 2.5 shows an alternative to the state giving zero voltage in the table. In the figure the dashed line represent the path the current flows from the neutral point to the load. It flows through two C4 capacitors, giving $\frac{V_{dc}}{2}$ potential, then through switch S1 and down the C3 capacitors. Since every capacitor is charged with the voltage $\frac{V_{dc}}{4}$ the potential is now lowered with $3\frac{V_{dc}}{4}$. The current the flows up through the diodes in parallel with the switches S_3' and S_2' and through capacitor C1 and then out to the load through switch S4 with the resulting potential 0 Volt.

Table 2.2: Switching states for a five level Capacitor Clamped Inverter. A "1" means turned on and "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0
0	1	0	1	0	1	1	0	0
$-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

As before with the NPCMLI only one switch need to be opened and one to be closed to change one state to another. This leads to that the inverter can be modulated at low (fundamental) switching frequency since a stepped sinusoidal waveform can be created when every switch is turned on and off only once per output frequency cycle. Also, as mentioned, the states shown in Table 2.2 are not the only states that put out these voltages, there are several switching states for all of the voltage levels, except the $\pm\frac{V_{dc}}{2}$ states. Depending on what state is chosen the capacitors can charge or discharge each other, making it possible to balance the charge in the capacitors with control methods[2]. Since the same current flows through all the active capacitors in a state, energy can be transferred from more charged to less charged capacitors, balancing the capacitors voltages between the capacitors that are conducting. If a method of using redundant switching states for voltage balancing is not applied there will be a capacitor voltage balance problem when transferring active power. However, if such a method is used the switching frequency may need to be raised for the balancing to be achieved properly [3]. The reason the capacitors voltages to get unbalanced while transferring active power some states are on during a longer time and the active capacitors gets discharged or charged more than others, much like in Figure 2.3. The unequal workload cause voltage unbalance but by using the redundant switching states the unbalances can be controlled. For pure reactive power transfer the CCMLI does not have any voltage balancing problem, which is also explained with Figure 2.3. Capacitors are charged and discharged equally during one cycle while transferring reactive power, like with the NPCMLI.

The amount of components for the CCMLI topology is as stated very similar to the NPCMLI, m-1 number of capacitors on a shared DC-bus and 2(m-1) switch-diode valve pairs, but with the difference that CC topology uses clamping capacitors instead of diodes. These capacitors do, as the diodes did, grow in numbers quadratically with the voltage level m, following the equation $\frac{(m-1)\cdot(m-2)}{2}$ [2], not counting the main capacitors on the DC-bus. Again the need for several components of the same sort and rating in series is needed because of the high voltage ratings, as for the clamping diodes in the NPCMLI. When the CCMLI is used in a three-phase setup it can, as the NPCMLI, share the DC-bus and only multiply all the other remaining components by three.

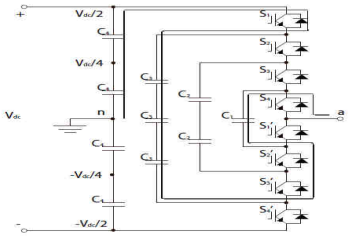

Figure 2.5: One example of a alternative switching state for the voltage 0. The dashed line represent how the current flows through the capacitors and switches out to the load.

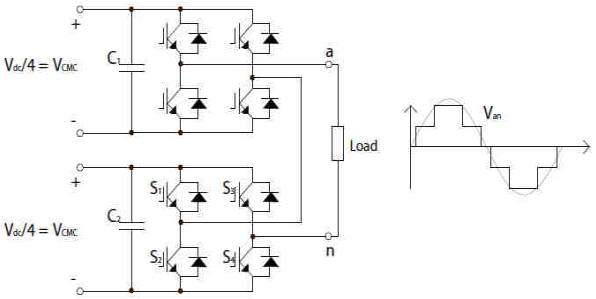

Figure 2.6: A five-level Cascaded Multicell Inverter

C. Cascaded Multicell Inverter, CMCI

A Cascaded Multicell Inverter (CMCI) differs in several ways from NPCMLI and CCMLI in how to achieve the multilevel voltage waveform. It uses cascaded full-bridge inverters with separate DC-sources, in a modular setup, to create the stepped waveform. In Figure 2.6 one phase-leg of a five-level Cascaded Multicell Inverter is shown. Each full-bridge can be seen as a module and it is only these modules that build up the CMCI topology. One full-bridge module is in itself a three-level CMCI, and every module added in cascade to that extends the inverter with two voltage levels. In Figure 2.6 there are two full-bridge modules creating the five different voltage levels available. Applications suitable for the CMCI are for example where photovoltaic cells, battery cells or fuel cells are used [3]. Such an example could be an Electric Vehicle there several power cells exists.

The total output voltage is the sum of the outputs of all the full-bridge modules in theinverter and every full-bridge can create the three voltages V_{CMC}, 0 and $-V_{CMC}$. To change one level of voltage in the phase output the CMCI turns one switches on (and one off) in one full-bridge module. For a full-bridge module to add the voltage V_{CMC} the switches $S_1$and S_4 are turned on, for $-V_{CMC}$ the switches S_2 and S_3 are turned on. When there is current _owing through the full-bridge the 0 voltage is achieved by turning on the two switches on the upper halves of the full-bridge (S_1 and S_3) or the two switches on the lower part (S_2 and S_4). Together with several

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full-bridges a stepped waveform can be generated. The maximum output voltage is $\frac{m-1}{2} V_{CMC} = sV_{CMC} = \frac{V_{dc}}{2}$ (and minimum voltage $\frac{m-1}{2}(-V_{CMC}) = s(-V_{CMC}) = -\frac{V_{dc}}{2}$), where m is the number of levels and s the number of full-bridge modules[2]. It should be noted that the CMCI is capable of putting out the total voltage source magnitude in both positive and negative direction while many other topologies can only put out half the total DC-bus voltage source magnitude. This is why the total sum of the DC-side voltages in Figure 2.6 is $\frac{V_{dc}}{2}$ and not V_{dc}, since it is still able to put out $\frac{V_{dc}}{2}$ to the output (like the other topologies). All full-bridge inverters that are connected can contribute with the same voltage, in a way making the topology very scalable. There is also the possibility to charge every modules with different voltages.

The sources in each full-bridge need to be isolated if the inverter is going to be implemented in a active power transfer application, for voltage balance reasons since there is no common DC-bus to recharge the sources energy content. However, since the CMCI uses separate energy sources it is well suitable for renewable energy or energy/fuel cell applications there every separate voltage source could be isolated [3]. A drawback for the energy/fuel cell applications is however that the sources must be charged individually or through the inverter. Still, the charge balance in the voltage sources needs to be controlled, for example in electric vehicle batteries, so that there is no voltage unbalance, but this can be done with balancing modulation methods. Balancing modulation methods will be investigated further in chapter 4. When adapted to pure reactive power applications the CMCI is self balanced, just as the NPCMLI and CCMLI, since the charge change over one cycle is zero [3] (right part of Figure 2.3). Since there is no common DC-bus to recharge the sources in the CMCI topology, balancing modulation strategies include prioritizing higher charged modules in modulation (see chapter 4) or activating two modules not needed for the output voltage level and let them balance each other (transferring energy from higher charged module to lower charged module). Two modules for balancing purposes are only available when the output voltage level is two levels lower than maximum (zero voltage level for the five-level MLI) or more. When two modules are available in this way one of the can be activated with positive voltage and the other with negative voltage. The resulting output voltage of these two modules is then zero but energy is transferred from the positive module to the negative module when current goes out from the inverter (and the other way around when current goes into the inverter). In this way two modules can balance each other when they are not needed for generating the output voltage.

Compared to the NPCMLI and CCMLI the CMCI requires fewer components, every voltage level requires the same amount of components. However, the number of sources are higher, for the phase-leg to be able to create a number of m voltage level s = $\frac{m-1}{2}$ sources are required [4]. The number of sources s is also equal to the number of full bridge modules. In turn, every full-bridge module has four diodes and four switches in turn giving the CMCI $4\frac{m-1}{2} = 2(m - 1) = 4s$ diodes and switches. When making a three-phase inverter with the CMCI topology the number if needed components needs to be multiplied by three for all components since there is no common DC-bus to share.

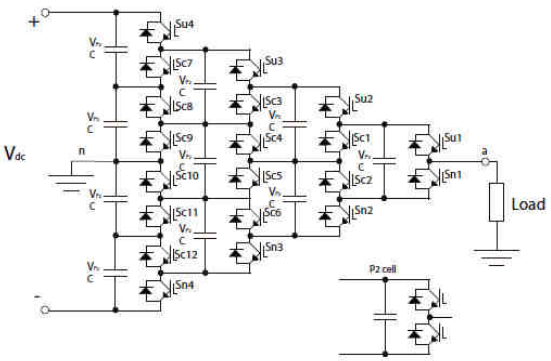

Figure 2.7: A five-level Generalized Multilevel Inverter

D. Generalized P2-cell Multilevel Inverter, GMLI

This far all the presented MLI:s all have a problem with voltage balancing when transferring active power. The Generalized Multilevel Inverter (GMLI), seen in Figure 2.7, does however not have the voltage balance problem since it is able to self balance its own capacitors without the need for extra circuits [5]. The NPCMLI, CCMLI and CMCI, among others, can also be derived from this generalized MLI topology [6]. The topology is based upon the use of simple two-level voltage cells, called P2 cells, which are connected in a triangular shape. Each P2 cell has two switch-diode pairs and one DC-capacitor that is charged with the value of $V_{P2} = \frac{V_{dc}}{m-1}$ (there m is the voltage level number). When one P2 cell is not used to achieve a certain voltage level it has one switch turned on to automatically balance the capacitor voltages[5], which one is decided depending on what switch in bordering P2 cell that is on. Figure 2.7 shows one phase leg for the generalized MLI, for three-phase two more of these circuits are needed in parallel. It is possible to share the DC-bus between phase-legs.

The two simplest voltage states for the GMLI, in this case a five-level GMLI, are the voltages $2V_{P2} = \frac{V_{dc}}{2}$ and $-2V_{P2} = -\frac{V_{dc}}{2}$. When all the upper switches (Su4, Su3, Su2, Su1) are on, the output voltage is 2VP2; and when all the lower switches (Sn4, Sn3, Sn2, Sn1) are on the voltage is $-2V_{P2}$. For all voltage states, except $\pm\frac{V_{dc}}{2}$, there are several combinations to choose from. The GMLI follow a couple of specific rules to decide which switches that should be on and o_, including which switches that should be on for the purpose of voltage balancing, in addition to that only one switch in a P2 cell is open at a time. The rules are as follows [5].

1. Each switch pole/P2 cell is independent
2. If one switch in a cell is on, the other is off
3. If a switch state is chosen, the other switches state can be determined by the two first rules.

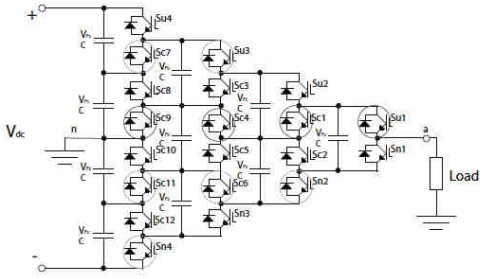

Figure 2.8: Generalized MLI in a switching state,

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switches in circles are turned on. In this case the output voltage is 0 since Sc9, Sc4, Sc1 and Su1 are turned on, represented with dark circles. The switches with lighter colored circles are on for balancing.

A switch pole is the two switches that exists in a P2 cell. These rules should be applied to the inverter after that switches for an output voltage state has been chosen. Figure 2.8 shows an example of a switching state there some switches are on for achieving the output voltage level and the rest of the switches that are on are balancing the capacitors voltages. To understand the automatic balancing for the GMLI topology note that, for instance, the switch Sc7 is switched on in Figure 2.8 for automatic balancing in the circuit and surrounding switches are turned off. This makes the DC-bus capacitor charge the cell capacitor close to Sc7 with the DC-bus capacitor voltage, $\frac{V_{dc}}{4}$, which is the voltage that all capacitors are charged with in this five-level case. During different voltage states other sets of capacitors can balance each other so that all capacitors are equally charged. The DC-bus capacitor, that can be assumed to be balanced, should be used properly in the balancing as well, as in the example above.

Even though the precise rules to control the inverter switches, holding the complexity back, it is clear from the figures that with increasing number of voltage levels the number of components required increase even more. To extend a m level GMLI inverter with one level, m P2 cells are needed. For two voltage levels, m+ (m+ 1) = 2m+ 1 P2 cells will be added, and so on. The number of P2 cells can be expressed with the sum

$$\sum_{n=1}^{m-1} n = \frac{m(m+1)}{2} - m$$

and as we can see in the figures, for every cell there is one capacitor, two diodes and two switches.

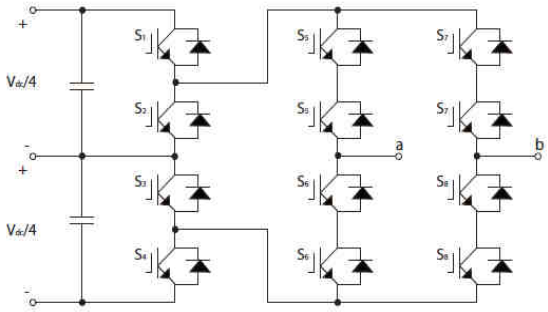

Figure 2.9: One phase-leg for a five-level Reversing Voltage Multilevel Inverter.

E. Reversing Voltage Multilevel Inverter, RVMLI

Compared with the four earlier chapters, which have presented popular and well documented multilevel topologies, the topology in this chapter, the Reversing Voltage topology, has not yet, as it seems, gained any great recognition. The Reversing Voltage (RV) MLI topology, displayed in Figure 2.9, was proposed during late 2008 [7] as a new topology to challenge the existing popular topologies, such as the NPCMLI. A great proposed advantage over the more popular MLI topologies, the NPCMLI and CCMLI, is the need for fewer components, but since components with equal ratings are used in this paper (in favor of comparison with other topologies) the number of components is not very low, as compared with if valves with different ratings would be used.

The basic method that the RVMLI uses in operation is to create a multilevel stepped voltage half-wave, only positive values, with a simple inverter with a low number of DC sources. The full-bridge connected to the first inverter can then reverse these positive half-wave voltages every half cycle to generate a complete sinusoidal voltage over the load. In this way, the components are used effectively, but if the circuits is going to withstand the voltages, under the assumptions that all devices of the same sort has the same ratings, additional valves are needed compared to requirements proposed in [7]. The full-bridge can also be controlled with low frequency since it is only supposed to reverse the voltage every half cycle, so the switch pairs in the full-bridge can be operated at the fundamental output voltage frequency [8]. The inner inverter could however be modulation at fundamental or high frequency independent of the full-bridge inverter modulation.

By operating the switches S_1 to S_4 a stepped positive voltage waveform is created and by opening either the switches S_5 and S_8 or S_6 and S_7 in the full-bridge a positive or negative voltage waveform is generated. Table 2.3 shows the different states for the multilevel positive half-wave inverter of the topology.

Table 2.3: Switching states for the five-level Reversing Voltage Inverter. A "1" means turned on and a "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$-\frac{V_{dc}}{2}$	1	0	0	1	0	1	1	0
$-\frac{V_{dc}}{4}$	0	1	0	1	0	1	1	0
0	0	1	1	0	1	0	0	1
$\frac{V_{dc}}{4}$	0	1	0	1	1	0	0	1
$\frac{V_{dc}}{2}$	1	0	0	1	1	0	0	1

Two advantages with the RVMLI are simpler controlling, since the modulation is divided in two parts (positive half-wave and reversing) and that it does not have a voltage unbalance problem if separate sources are used, as proposed in [7]. It is however true for several topologies that separate sources can solve the voltage unbalance problem. If separate sources are not used, balancing will have to be achieved by balancing the workload between the sources, since there is also one more state to create the $\frac{V_{dc}}{4}$ voltage (switches S1 and S3 on instead of S2 and S4). If workload is modulated properly it can be chosen from which source energy is to be transferred to or from during the $\pm\frac{V_{dc}}{4}$ voltage states and in that way the sources can be held balanced. As for the CMCI the RVMLI is capable of putting out the full range of its DC-side voltage, dividing the need for the DC-side voltage by two for the same output voltage compared to other topologies, such as the NPCMLI.

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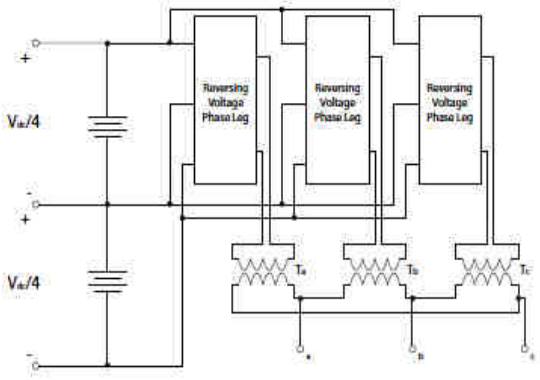

Figure 2.10: A three phase setup with five-level RVMLI phase-legs and transformers on each phase

For a number of voltage levels m the topology needs $(m-1)+2(m-1) = 3(m-1)$ main switches and diodes per phase and also $\frac{m-1}{2}$ isolated supplies [7] and/or DC capacitors. The reason for the high number of components in the full-bridge is that every phase leg in the full-bridge must be able to withstand the voltages from the multilevel inverter phase-leg. No clamping diodes or flying capacitors are needed. However, even though the number of components are low, a transformer is required for isolation on the load side for each phase if the low number of sources is going to be valid [8], see Figure 2.10. This could however also be applied to other topologies. The importance of the use of transformers is also dependent on the application.

F. Modular Multilevel Inverter, M2I

The Modular Multilevel Inverter (M2I), seen in Figure 2.11, is a newer topology first introduced in 2002 [17]. It uses a modularized setup of submodules, essentially halfbridges, which are connected or bypassed to generate a certain output voltage level. Every phase-leg is composed of two arms where each arm has a number of *n* submodules. In turn, in every submodule there is a DC-capacitor charged with the voltage $V_{M2I} = \frac{V_{dc}}{m-1}$. Each arm can then generate the maximum voltage of $\pm n*V_{M2I} = \pm V_{dc}$, where the modules in both arms are connected or bypassed to create a AC output voltage. So for a number of voltage levels m the inverter needs m-1 = n number of submodules per arm, so 2(m-1) = 2n submodules per phase-leg. Compared to the somewhat similar CMCI topology the modules in this M2I topology can only put out two voltages, VM2I or 0. This explains the need for two arms in every phase-leg. The M2I topology does not need shared DC-capacitors in a DC-bus, but does however require a DC-bus for circulating currents. These currents can however also circulate through other phase-legs. The two inductors, one in each arm in a phase-leg, are there to take up the voltage difference when modules are switched in and out.

To activate a certain submodule in an phase-leg arm to make its voltage source contribute to the output voltage the switch S1 is switched on and S2 is switched off. To bypass a submodule the switches S1 is turned off and S2 is turned on in that certain submodule. The arm in which a submodule is to be connected is determined by if the wanted voltage is positive or negative and which submodule in the arm is determined by the balancing modulation. The balancing modulation is the program that chooses which modules that are to be activated for each state to achieve voltage balance in all modules. To keep the sources in the submodules balanced the order in which they are connected can be changed. If, for instance, one submodule has more charge stored in its capacitor it can be prioritized to be activated first or last, depending on current direction, to balance the submodule voltages. The M2I topology hence has a redundant setup of switching states. Some switching state examples for achieving the voltage levels in this five-level M2I can be seen in Table 2.4. Note that during any moment, half the modules are connected and half the modules are bypassed. This is necessary since the sum of all connected modules in a phase-leg must be V_{dc}.

Component requirements for the M2I topology is mostly dependent on the number of submodules, and hence the number of voltage levels, since there is only the inductors in the topology setup that is independent of the number of levels. Every submodule is composes of a half-bridge and a DC-capacitor, so for every submodule there is two switches, two diodes and one capacitor. Additionally, for every phase-leg there is two inductors for the phase-leg arms. The inductors, seen close to the midpoint in the phase-leg in Figure 2.11, are there to take up the voltage difference between states. Also, each switch in the M2I submodules must be able to withstand at least the submodule capacitor voltage, VM2I . Since the voltage spanning over both arms is V_{dc} and the number of submodules in the arms, as a function of number of voltage levels, is m-1 the voltage that a switch must be able to withstand described with the total DC voltage is $\frac{V_{dc}}{m-1}$.

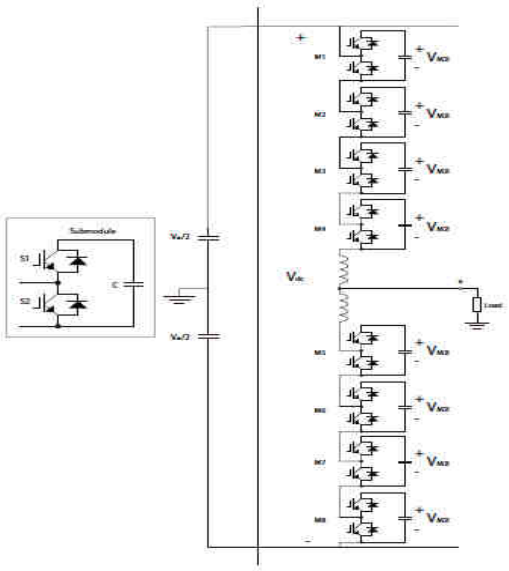

Figure 2.11: One phase-leg of a five-level Modular Multilevel Inverter

Table 2.4: M2I switching states examples. A "1" means that a submodule is inserted (switch S1 on) and a "0" means that it is bypassed (switch S2 on).

V_{load}	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
$\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1
$\frac{V_{dc}}{4}$	1	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1
$-\frac{V_{dc}}{4}$	1	1	1	0	0	0	0	1
$-\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0

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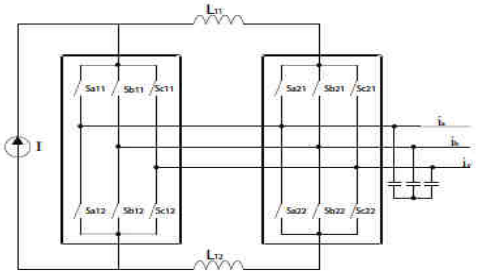

Figure 2.12: A three-phase five-level Generalized Current Source Inverter

G. Generalized Multilevel Current Source Inverter, GMCSI

The topologies presented so far have all been inverters with voltage sources, so called Voltage Source Inverters (VSI). Even though Multilevel VSI:s are the most popular topologies [3] there do exist multilevel Current Source Inverters (CSI). The concept of a multilevel CSI is to use one or more current sources instead of voltage sources and with the help of power electronics inject levels of current to a load. In this paper the Generalized Multilevel Currents Source Inverter (GMCSI) from [9] will be presented, displayed in Figure 2.12.

The GMCSI is a three-phase topology that consist of a number of "current source six-valve modules", see the valves within dashed lines in Figure 2.12. In addition there are also m-3 positions with inductors to smooth the DC-side current and to divide its source into different current ratings [9]. Only one current source is needed. As with many of the other MLI topologies, one of the advantages with the GMCSI topology is that it can eliminate the use of transformers in some high power applications. Also the modularized configuration is advantageous and the topology is not as component heavy as some other topologies [9].

Table 2.5: Examples for some GMCSI switching states

i_a	i_b	i_c	Switches on
0	I	-I	Sb12,Sb22,Sc11,Sc21
$\frac{I}{2}$	-I	$\frac{I}{2}$	Sa11,Sb12,Sb22,Sc21
I	-I	0	Sa11,Sa21,Sb12,Sb22
I	$-\frac{I}{2}$	$-\frac{I}{2}$	Sa11,Sa21,Sc12,Sc22

One problem with the GMCSI, comparable with the voltage unbalance problem in some of the VSI:s, is that there can be a current unbalance in the smoothing inductors. This problem can however be solved with the use of redundant switching states [9]. The number of switching states for a GMCSI can also be calculated by the number of modules n ($n = \frac{m-1}{2}$ as mentioned above) with the equation

$$N_c = 3^{2n} \qquad (2.1)$$

where N_c is the number of switching states. For the five-level GMCSI, $N_c = 3^{2*2} = 81$,meaning 81 switching states on five levels for three phases. Some of these states is shown in Table 2.5. The reason for the inductor current unbalance is the voltage across the inductors. Depending on if the voltage is positive or negative the current through the inductors will ramp up or down from its supposed value. By changing states in a proper way the inductor currents can be held on a balanced level.

The inductors also have different amounts of current flowing through them and the amount of current is dependent of the inductors position. For every valve module that is passed the current amplitude drops $\frac{I}{n}$ since the amount of current that goes through every closed switch (in every module) is $\frac{I}{n}$. Also, only one switch in the upper half of a valve module and one switch in the lower half of a valve module can be switched on at any moment [9]. This also means that the current rating of a valve should be at least $\frac{I}{n} = \frac{2I}{m-1}$. Since different amounts of current flow through the inductors depending on their position it is necessary to add inductors in parallel closer to the source if components with the same current rating are to be used. For an GMCSI with m number of current levels the inverter is composed of $\frac{m-1}{2}$ valve modules (within the dashed line in Figure 2.12), which all contain six switches. There are also m-3 positions where inductors should be placed. With inductors with equal current rating the number of inductors is $\frac{m-1}{2}(\frac{m-3}{2}-1)$. For the seven-level GMCSI this would mean two inductors in parallel closest to the source (on each side, top and bottom) and one inductor at the second inductor position. For a nine-level GMCSI three inductors in parallel would be in the first position followed by two and one inductor.

III. MODULATION STRATEGIES

When it comes to multilevel inverter modulation there are basically two groups of methods: modulation with fundamental switching frequency or high switching frequency PWM [2]. For both cases a stepped output waveform is achieved, but with the high switching frequency methods the steppes are modulated with some sort of PWM. Independent of switching frequency choice there are, however, also space vector methods to choose from.

A. PWM for two-level inverters

Ordinary PWM modulation for two-level inverters is accomplished through comparison between a reference wave and a triangular carrier wave. The reference wave have the frequency and amplitude wanted for the output voltage signal and the triangular carrier wave has the amplitude of half the DC input voltage, in an simple ordinary case, and its frequency is dependent on application but must be higher than the reference wave frequency. In electric power application the carrier wave frequency is often in the range of kHz. The reference wave frequency decides how often the switches in the inverter changes state, every time the triangular carrier wave crosses the reference wave the switches turn on or off. A plot of the ordinary two-level PWM reference, carrier wave and output voltage can be seen in Figure 3.1. If the carrier wave crosses the reference so it becomes higher than the reference the top switch turns off and bottom switch turns on in the twolevel inverter (see Figure 1.1) so that $\frac{V_{dc}}{2}$ becomes the output. When the carrier wave crosses the reference again, now getting lower than the reference, the switches change state and the output becomes $-\frac{V_{dc}}{2}$. When the reference is positive the output voltage signal will be $\frac{V_{dc}}{2}$ for the majority of the time resulting in a positive output AC signal following the reference. An straightforward example is if the reference wave is constant at zero voltage, the carrier wave would then cross it upwards and downwards with the same time between every crossing, making $\frac{V_{dc}}{2}$ and

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$-\frac{V_{dc}}{2}$ being the output for equal time, each cycle. This leads to that the average output voltage over one carrier wave period becomes zero.

B. PWM for multilevel inverters

Multilevel PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave, much like in the two-level PWM case. To reduce harmonic distortions in the output signal phase-shifting techniques are used [2]. There are several methods that change disposition of or shift multiple triangular carrier waves. The number of carrier waves used is dependent to the number of switches to be controlled in the inverter.

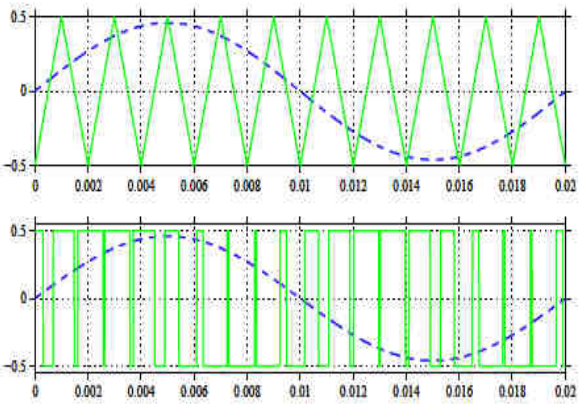

Figure 3.1: PWM reference (blue dashed) and triangular carrier (green solid) wave in upper plot and output voltage (green solid) eave in lower plot

In addition to the two sinusoidal carrier wave modulation methods presented further down there are also two more well known alternative methods that will not be discussed in this paper: Alternative Position Opposition Disposition (APOD) and Phase Opposition Disposition (POD) [10].

B.1 Phase Shifted Carrier PWM

The Phase Shifted Carrier PWM (PSCPWM), Figure 3.2, is a multicarrier modulation strategy that has all carrier waves phase shifted from each other. It is the standard modulation strategy for the CMCI topology [10] but is not exclusively for that topology.

For a CMCI with n number of full-bridge modules in each phase-leg there are also n number of triangular carrier waves. There is one triangular carrier wave for each fullbridge module, phase shifted with $\frac{180^{\circ}}{n}$ in between them, with amplitudes the magnitude of the total DC voltage. The magnitudes for the carrier waves are modulated by the actual voltage level in the appropriate module. For the _ve-level CMCI with two modules there are two triangular carrier waves, one for each module, see Figure 3.2. The modules create the two voltages in Figure 3.3 with PSCPWM modulation. There are also two reference waveforms for the two legs in each inverter modules that are phase shifted 180° from each other, as can be seen in Figure 3.2. Both reference waves are compared with both carrier waves, one reference wave is for modulation of the left full-bridge module leg switches (dashed reference wave) and the other reference wave to modulate the right full-bridge module leg switches (solid reference wave). The first triangular wave in Figure 3.2 is compared with the upper output voltage plot in Figure 3.3 (and the second triangular with the lower voltage plot). Close to 2ms in the plots it can be seen that the first triangular wave crosses one reference wave downwards, controlling the right leg switches of the modules, turning that modules output voltage from 0kV to -0.5 kV. Closely after the second carrier wave crosses the same reference wave (the one that controls the right leg switches in the modules) upwards turning the output voltage from -0.5 kV to 0 kV. Comparisons with the other reference wave works in the same wave, but then controlling switches in the modules left legs. As the plots suggests the two modules share the workload for all levels, no module is strictly connected to one voltage level in the output. For the CMCI this strategy cancels all carrier and sideband associated harmonics up to the 2nth carrier group [11].

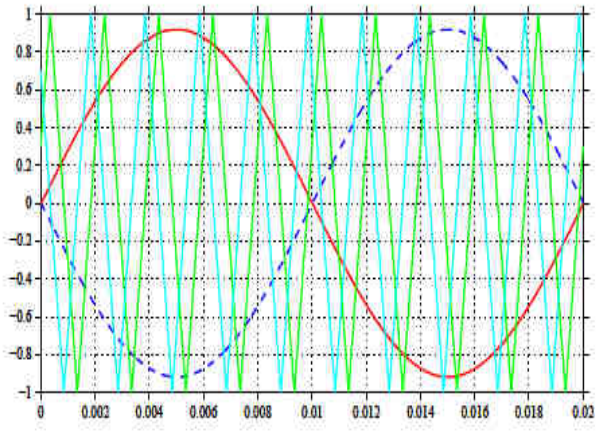

Figure 3.2: The carrier and reference waves for a five-level CMCI with PSCPWM, two reference waves and two triangular waves (one for each module)

B.2 Phase Distortion PWM

In Phase Distortion PWM (PDPWM), Figure 3.4, all carrier waves are in phase. A great acknowledgment for this technique is that it is generally accepted as the method that creates the lowest harmonic distortion in line-to-line voltage [12].

When used for an NPCMLI with m number of voltage levels, m-1 number of triangular carrier waves are used. These carrier waves have the same frequency and are arranged on top of each other, with no phase shift, so that they together span from maximum output voltage to minimum output voltage [11]. The carrier waves amplitudes should be modulated with aspect of the current voltage magnitude for each respective voltage level, each carrier wave is connected to a specific output voltage level. If the carrier waves are not modulated in this way the correct output voltage will not be achieved if the sources voltage levels change from their supposed value (get unbalanced). If the sources voltage amplitudes change without that the carrier waves are modulated with that change the correct output voltage will not be generated during the during the correct time spans. When one carrier wave is crossed by the reference the output wave steps one level up or down with a switch transaction. One carrier wave hence modulates the use of one voltage state. Only one level is modulated at any time, as can be seen in the in Figure 3.4, since the reference only crosses one carrier at any level. The output voltage from the PDPWM modulation with a five-level NPCMLI is shown in Figure 3.5. The carrier waves should be modulated with aspect of the current voltage magnitude for each respective voltage level.

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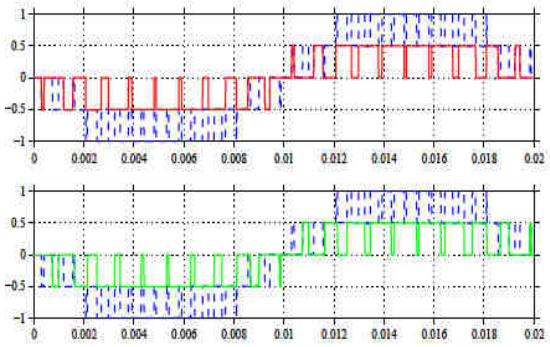

Figure 3.3: The two module voltages, one in each plot, together with the achieved total output voltage (blue dashed line in both plots)

Phase Distortion PWM is also the proposed control method for the RVMLI [8] but can be used with other topologies as well. For the CMCI the PDPWM modulation is built up of m-1 carrier waves, two for each full-bridge module, one below zero and one above zero for every module. Each module then modulates one voltage level. Which level one full-bridge module modulates can be changed for balancing purposes. For the five-level CMCI this could mean that the module with highest charge within its source is modulated by the carrier waves two and three in Figure 3.4, if counting the carrier waves from top to bottom. The other module, with lower charge, would then be controlled by carrier waves one and four. Since waves two and three are closest to zero the first module, with higher charge, will be connected to the load first every half cycle, for both positive and negative output voltages. This will lead to a higher workload for this module. If which module contains the most charge change, the modules can change which carrier waves that modulate them with each other. More generally, the two triangular waves closes to zero (one wave with positive voltage and one with negative voltage) can control the module with the highest charge if active power is to be transferred. The positive carrier then modulated the full-bridge modules left leg for positive output voltages and the negative carrier the right leg for negative output voltages. Other modules should be controlled by two carrier waves further away from zero, one from each side of zero voltage at the same position (second wave above and second wave below zero, for example). The carrier waves amplitudes should be modulated by the voltage level in the full-bridge module it controls, much like with the carrier wave modulation for PSCPWM, so that correct output voltages are generated during the correct time spans.

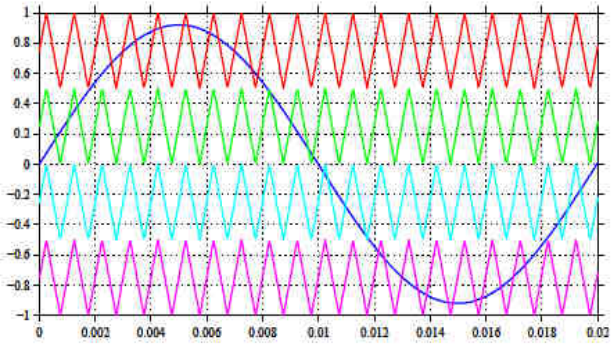

Figure 3.4: The reference (cosine) and carrier waves (triangular) for a five-level Npcmli or cmci with Pdpwm.

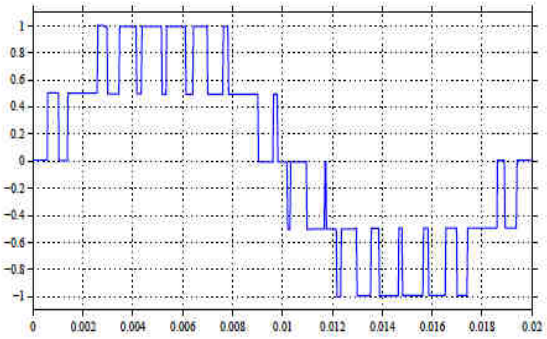

Figure 3.5: The output voltage for a five-level NPCMLI with PDPWM.

C. Space Vector Modulation and Space Vector Control

Space Vector Modulation (SVM) is a high frequency modulation alternative to PWM, where one big difference is that SVM must be used with a three-phase system. In SVM, the three reference phases are transformed into one reference vector which is placed inside a Space Vector Diagram, see Figure 3.6. Depending on the three phases amplitudes the vector in the diagram will end up somewhere in one of the diagrams triangles. Every corner of the diagram represents a state for the three-phase inverter, where the state number represent the wanted level for each phase-leg. The states for the three corners in the triangle that the vector is inside are modulated, each state on for a specific time, so that the vector is recreated by the inverter in the form of a mean value of the three used vectors in the diagram. The left part of Figure 3.6 shows the Space Vector Diagram for a three-phase two-level inverter. In this case the voltage reference vector is inside the upper right triangle of the diagram. This means that the inverter will use the vectors 110, 100, and 111 or 000 to create output voltage like that the reference represents. Every number in a state nnn (for example 110) is connected to a phase-leg and represent the level wanted, 1 for positive voltage and 0 for negative voltage. The same applies for a multilevel Space Vector Diagram but the states includes more level, a state could for instance be 302 which would mean that one phase leg should put out voltage level 3, one leg voltage level 0, and one leg voltage level 2 for a calculated amount of time. A five-level Space Vector Diagram is shown to the right in Figure 3.6. The three vectors that would be used to recreate the reference in the multilevel Space Vector Diagram in the figure (if lowest level is 0 and highest 4) are 210, 220 and 320. Space Vector Modulation can be used with any multilevel inverter since its vector diagram are universal and has relative easy hardware implementation by a Digital Signal Processor [2]. However, with higher number of voltage levels the complexity of choosing switching states increases since the redundancy of switching states increases as well.

Space Vector Control (SVC), a low (fundamental) frequency space vector modulation method, does not, contrary to SVM, generate the desired mean load voltage value in every switching interval but for inverters with a higher number voltage levels the errors will be small in comparison to the reference vector [2]. SVC may therefore be adequate for inverter with higher number of voltage levels.

D. Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a low switching

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frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage. With the help of Fourier Series analysis the amplitude of any odd harmonic in the output signal can be calculated. Usually the switching angles are chosen so that the fundamental is set to the wanted output amplitude and the other harmonics to zero, see Figure 3.7. The switching angles must however be lower than $\frac{\pi}{2}$ degrees and for *a* number of switching angles *a* harmonic components can be affected, where *a-1* number of harmonics can be eliminated[2] (one angle to set the fundamental). If angles were to be larger than $\frac{\pi}{2}$ an correct output signal would not be achievable. For an inverter with m levels a = $\frac{m-1}{2}$. Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. For a five-level inverter *a = 2*, so there are two switching angles available and *a-1 = 1* angles can be used for harmonic component elimination.

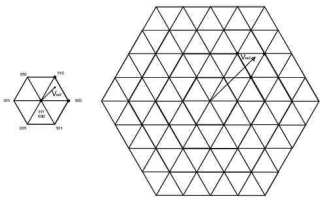

Figure 3.6: A two-level Space Vector Diagram, to the left, and a five-level Space Vector Diagram, to the right

In Figure 3.7 the first angle, $\alpha 1$, is set to modulate the fundamental signal amplitude the second angle, $\alpha 2$, is set to eliminate a chosen harmonic distortion. The Fourier Series equations for these signals are the following.

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{2}\cos\alpha 1 + \frac{V_{max}}{2}\cos\alpha 2 \quad (3.1)$$

$$0 = \cos(n * \alpha 1) + \cos(n * \alpha 2) \quad (3.2)$$

$$m_i = \frac{V_{ref}}{\sqrt{2}V_{max}} \quad (3.3)$$

The variable *n* is in these equations is the number (multiple of the fundamental frequency) of the harmonic that is to be eliminated. For every switch angle available one cosine term *i* added to each equations and there are also as many equations as there are switching angles. So for a situation with *a* number of switching angles there are *a* number of equations with a number of cosine terms. As for this five-level inverter case there are two firing angles, two equations and two cosine terms in every equation. For a seven-level inverter the equation setup would instead be as the following. Variables n_1 and n_2 are the numbers of the two harmonics to be eliminated.

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{2}\cos(\alpha 1) + \frac{V_{max}}{2}\cos(\alpha 2) + \frac{V_{max}}{2}\cos(\alpha 3) \quad (3.4)$$

$$0 = \cos(n_1 * \alpha 1) + \cos(n_2 * \alpha 2) + \cos(n_3 * \alpha 3) \quad (3.5)$$

$$0 = \cos(n_2 * \alpha 1) + \cos(n_2 * \alpha 2) + \cos(n_2 * \alpha 3) \quad (3.6)$$

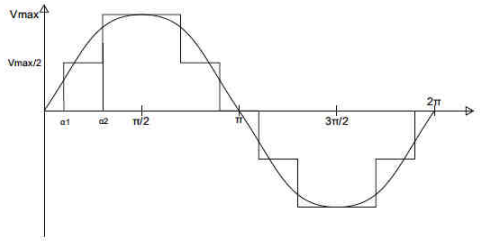

Figure 3.7: Switching with angles determined by Selective Harmonic Elimination for a five-level inverter

Table 3.1: Component Requirements for the Topologies for a three-phase setup. The voltage/current level is represented by m. DC-buses are not shared between the phases.

Topology	NPCMLI	CCMLI	CMCI	GMLI	RVMLI	GMCSI	M2I
DC-bus cap./Isolated sources	3(m-1)	3(m-1)	$3\frac{m-1}{2}$	$3\frac{(m-1)(m-2)}{2}$	$3\frac{m-1}{2}$	1	6(m-1)
Main diodes	6(m-1)	6(m-1)	6(m-1)	$6\frac{(m-1)(m-2)}{2}$	3(3(m-1))	0* $6\frac{m-1}{2}$**	12(m-1)
Main switches	6(m-1)	6(m-1)	6(m-1)	$6\frac{(m-1)(m-2)}{2}$	3(3(m-1))	$6\frac{m-1}{2}$* $6\frac{m-1}{2}$**	12(m-1)
Clamping diodes	3(m-1) (m-2)	0	0	0	0	0	0
Clamping cap.	0	$3\frac{(m-1)(m-2)}{2}$	0	0	0	0	0
Smoothing ind.	0	0	0	0	0	$\frac{m-1}{2}\frac{m-1}{2}+1$	6
Transformers	0	0	0	0	3***	0	0

*GMCSI with GTO switches

**GMCSI with IGBT switches and parallel diode (not used in plots and comparisons)

***Three transformers as in one transformer for each phase in a three-phase setup

IV. APPLICATIONS

When the number of levels is greater than three, both the diode-clamped and cascaded multilevel inverters have equivalently separate dc sources for each level in order to enable power conversion involving real power such as in motor drives. On the other hand, the cascaded multilevel inverter is best suited for harmonic/reactive compensation and other utility applications.

A. Hybrid Electric Vehicle Application

Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV) are becoming more and more popular and they are more than likely to be a part of a more sustainable society. Depending on EV/HEV configuration, the power train need one or more converters/inverters to feed power for propulsion. The electric system of a EV/HEV uses series and parallel connected battery cells as power source. The voltage level of these batteries needs to be controlled with extra circuitry so they are equally charged. High efficiency, to achieve long driving range, is important but compact design and light weight of the power electronics, and other devices, are also essential. There are also EMI regulations. A simple example of a EV electric power train setup can be seen in Figure 4.1.

An MLI topology suitable for implementation in a HEV should, with the aspects above in mind, be able to deliver an alternating voltage with low losses and take advantage of the multiple battery cells setup used in EV:s/HEV:s with weight and efficiency prioritized. Real power transfer is important for this case so the chosen topology should have no problems with or effective solutions for voltage unbalances. If the inverter in itself could control the voltage levels of the sources that would be an advantage. In line with efficiency and light weight there is also need for low EMI, preferably without filters, so low distortions is an important quality for the MLI topology.

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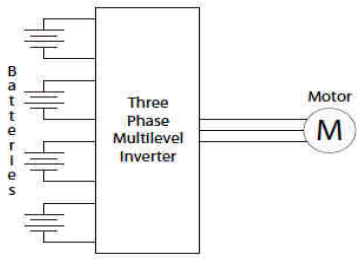

Figure 4.1 Hybrid Electric Vehicle/Electric Vehicle power train

With aspect to these design requirements for an application with several battery cells as power source, the CMCI topology has been chosen for the EV/HEV application simulation in this work. Dividing the batteries into several isolated DC sources, as shown in Figure 3.8, real power can be transferred without voltage unbalance problems when correct modulation is applied. This makes the CMCI suitable for this application. Charge balance in the batteries must however be controlled but since the CMCI topology can control the sources workload with the modulation, there is no need for extra balancing circuits. This leads to lower weight and higher efficiency. Another advantage with the topology is that low amounts of components are needed (leading to lower weight), compared with other multilevel topologies. The topology setup can also be combined with the battery cell setup where the cells in series can be for build up one phase-leg, taking advantage of the topologys modular setup, and cells in parallel can build up several phases. With enough voltage levels the CMCI should also be able to produce an output voltage with low distortions. The ability to switch at fundamental frequency also leads to high efficiency, extending the driving range for the vehicle (this is however, as stated, not a special feature for the CMCI).

Another topology that could have been used for these simulations is the M2I topology. The M2I topology could also make good use of its modular design and balancing methods. However, even though the M2I uses a low number of components the CMCI needs even fewer and the M2I also needs more sources than the CMCI. Because of this the CMCI was chosen over the M2I.

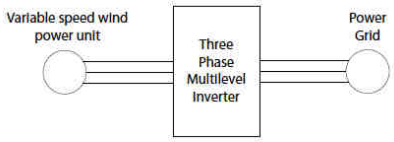

Figure 4.2: Power Grid Application example

B. Electric Power Grid Systems

In line with more decentralized power generation and smarter power grids with more renewable power sources new requirements follows. DC/DC, AC/DC and AC/DC conversion is required for several applications such as HVDC-transmission application and back-to-back configurations for asynchronous grid connection [3], for example for connecting wind farms with the power grid, see Figure 4.2. There is also need for reactive power compensation and power outage/voltage dip compensation. Low EMI and high efficiency are also among the requirements. For power grid applications a common DC-bus is necessary when power is to be transferred.

An MLI topology suitable for Electric Power Grid applications should be able to be used in compensations applications and FACTS but also have rectifying capability so that it may be used for HVDC-transmission and similar applications. It would also be preferred if the use for high power transformers could be minimized or eliminated. For some applications there is however no need for transformer elimination, for example HVDC where transformers exists anyway. For some of the applications there is active power transfer and chosen application need a solution to the voltage unbalance problem for these cases. The MLI topology should also have high efficiency and be able to produce low EMI and other distortions to avoid large filters. Chosen available topology should also be able to transfer both active and reactive power, however not necessarily at the same time, and must also have a common DC-bus to be suitable for power grid system applications.

For the Power Grid case several of the presented topologies are suitable for one or more of the interesting applications, for example reactive power compensation [3]. The three biggest topologies, the NPCMLI, CCMLI and CMCI, can all be used in reactive power compensation without voltage unbalance problem but only the NPCMLI and CCMLI have a common DC-bus and are possible in back-to-back configurations. The GMLI can auto-balance the capacitor voltage but uses the most components. The RVMLI uses the least amount of components and was proposed to be used in HVDC [7] but it require isolated sources and transformers for balanced operation.

With aspect to industrial popularity [13], design simplicity, suitability for back-to-back and reactive power compensation the NPCMLI have been chosen for simulation for the Electric Grid System case in this work. With the proposed vector control method in [14] and [15] the capacitor voltage unbalance can be controlled which makes the NPCMLI a attractive choice. The NPCMLI can transfer both reactive and active power, as mentioned, have a common DC-bus and the topology itself have no need for transformers. Several balancing methods are known for the NPCMLI and the ability to function with low switching frequency leads to high efficiency. Also, the multilevel setup creates low distortions, lowering need for big filters.

V. FUTURE TRENDS

By looking at the number of papers published in recent years, it is easy to conclude that multilevel inverter research and development activities are experiencing an explosive rate of growth. A trend of having more and more multilevel inverters is obvious. Although this paper has focused on multilevel inverter circuit topology, control, and applications, there is other research and development in related areas, such as high-voltage high-power semiconductor devices, sensors, high-speed DSPs, thermal management, and packaging.

Based on the progress of semiconductor devices and advanced circuit topologies, future trends can be observed in the areas of advanced high voltage high power semiconductor devices, optical fibres for sensors and controls, thermal management and distributed energy systems.

VI. CONCLUSION

This paper has provided a brief summary of multilevel inverter circuit topologies and their control strategies.

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Different applications using different inverter circuits were also discussed. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. The intention of the authors was simply to provide groundwork to readers interested in looking back on the evolution of multilevel inverter technologies, and to consider where to go from here.

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