Design and Operation of 4X1 Low Power Multiplexer using Different Logics

Yalla Hareesh, Yelithoti Sravana Kumar

Abstract: ***Low power and high speed digital circuits are basic needs for any of digital circuit. Multiplexer is a basic circuit for any digital circuit. In this paper, different techniques of multiplexer designs like Complementary CMOS, Transmission gate, Pass transistor logic, Dual Pass transistor logic styles and Gate Diffusion Input has been introduced and their comparison on the basis of power, delay and Area (number of transistor) is done. A low power Multiplexer has been introduced which consumes least power as compare to above mentioned logic but have more delay as compare to other ,On the basis of these analyses it is concluded that proposed multiplexer is better technique for designing an low power low area Multiplexer design but it has high delay as compare to other Multiplexer.***

Keywords: CMOS, DPTL, PT, TG, GDI

I. INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing Combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles [2].

This paper analyzes 4-to-1 multiplexer using complementary CMOS, Transmission gate, Pass transistor logic, Dual Pass transistor logic styles and Gate Diffusion Input. These implementations are compared based on the basis of transistor count, power dissipation, and delay A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of inputs has n select lines, which are used to select which input line to send to the output that is why it is also called a data selector. Multiplexer can also be used to implement any combinational circuit. So by simplifying design of multiplexer, design of many combinational circuits can be simplified [5]. Fig.1 and fig.2 show the block diagram and truth table for 4-to-1 multiplexer given below [5].

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II. LOW POWER TECHNIQUES

2.1. Conventional CMOS

In conventional or complementary CMOS logic gates are made up of an pmos pull-up and a nmos pull down logic network. CMOS logic style has an advantage of robustness against voltage scaling and transistor sizing .It has high noise margins and operates reliably at low voltages. Connection of input signals to transistor gates only, facilitates the usage and characterization of logic cells. The complementary transistor pair makes the layout of CMOS gates efficient and straightforward. The major disadvantage of CMOS is substantial number of large PMOS transistors which results in high input loads.

2.2. Gate Diffusion Input (GDI)

Apart from Conventional CMOS design, another alternative low power and area efficient technique is GDI technique. A basic GDI cell consists of four terminals- D (common diffusion of both transistors), N (outer diffusion node of nMOS transistor), P (outer diffusion node of pMOS), G (common gate input to both pMOS and nMOS transistors). Depending on the circuit structure and its mode of operation P, D and N can be used as either inputs or outputs.

2.3. Dual Pass Transistor Logic (DPTL)

The powerful configuration in CMOS technology is Dual Pass Transistor Logic (DPTL). Regardless of input signal-swing variation, DPTL buffers have the ability to generate standard CMOS levels. A basic DPTL structure consists of pMOS and nMOS transistors connected in parallel. Dual logic function in DPTL is generated by exchanging NMOS and PMOS, VDD and GND.

2.4. Pass-Transistor Logic style (PT)

The pass-transistor logic reduces the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source drain terminals. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation [7, 8]. Several pass-transistor logic styles such as NMOS Pass Transistor Logic, CMOS Transmission gate, and pass transistor logic(PTL) are considered to implement4-to-1multiplexer [3, 5, 6]. Among all these NMOS Multiplexer is optimal. It uses two NMOS transistors and these two-pass transistors at the input select which signal to propagate. The logic levels will be deteriorated by the pass transistor. The threshold voltage of both pass-transistors should be identical for accurate operation. Figures in the simulation section represent design of 4-to-1 multiplexer using several logic styles.

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2.5. Transmission gate(TG) Logic Style

In this logic style N and P devices with sources and drains connected in parallel. V_g is the control signal for the N device, V_{gc} (complement of V_g) is the control signal for the P device. So When V_g is high (at V_{dd}) and V_{gc} is therefore low (at Gnd), the NFET and PFET are both ON [4]. (Depending upon the devices' source potentials, one may be ON more strongly than the other.) The switch is therefore CLOSED and V_{out} will be the same logic level as V_{in}. When V_g is low (at Gnd) and V_{gc} is high (at V_{dd}), both devices are OFF. The switch is therefore OPEN and V_{out} will be independent of V_{in}. A 4-to-1 multiplexer can be implemented using transistors by this logic style.

III. DESIGNING OF 4X1 MUX USING DIFFERENT LOGICS

In this paper different logic styles complementary CMOS, Transmission gate, Pass transistor logic, Dual Pass transistor logic and Gate Diffusion Input were used to design 4 to1 multiplexer. These multiplexers were designed on S-edit of Tanner tool on 45nm technology and simulated on T-edit with 1v power supply. Figures shows schematics of multiplexers designed using two logic styles.

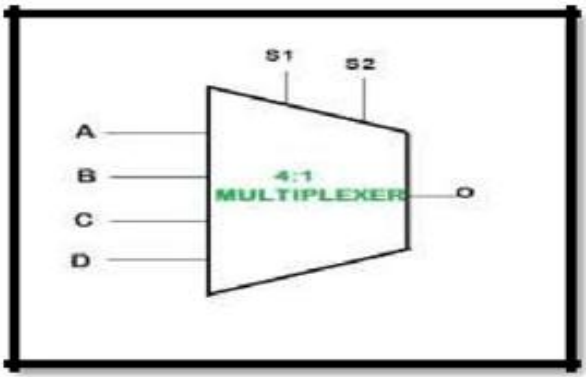

Fig1: 4X1 Multiplexer

TABLE 1: Truth Table of 4X1 Mux

SELECTI		INPUTS				O/P
S2	S1	A	B	C	D	Y
0	0	1	0	0	0	A
0	1	0	1	0	0	B
1	0	0	0	1	0	C
1	1	0	0	0	1	D

3.1. Conventional CMOS

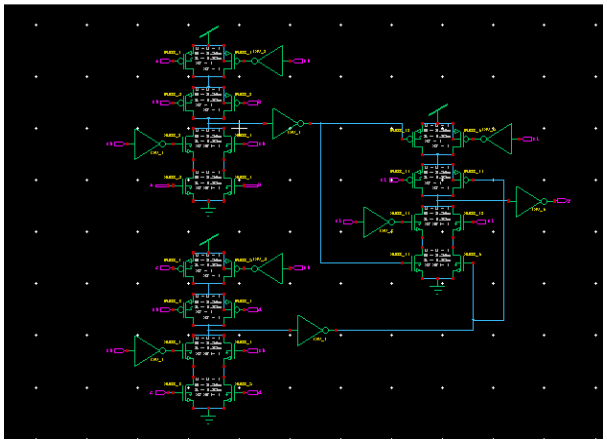

Fig 2: 4X1 MUX using CMOS

From fig we can say that the CMOS technique utilizes more as large number of transistors are used resulting in large power dissipation.

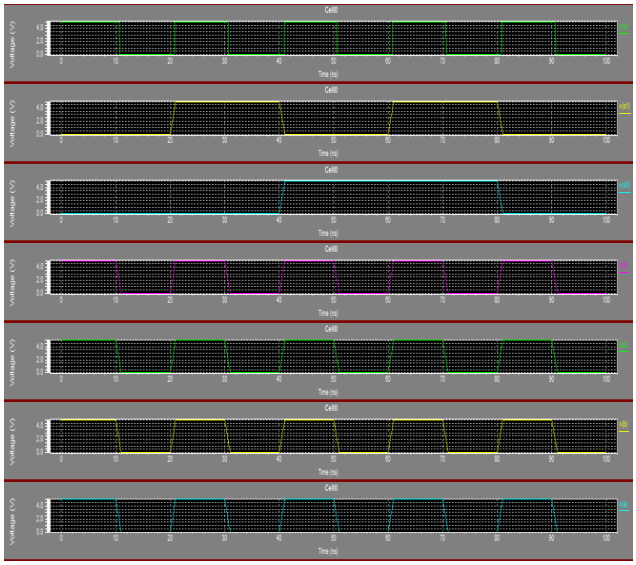

Fig: 3 CMOS Waveform

3.2. Gate Diffusion Input (GDI)

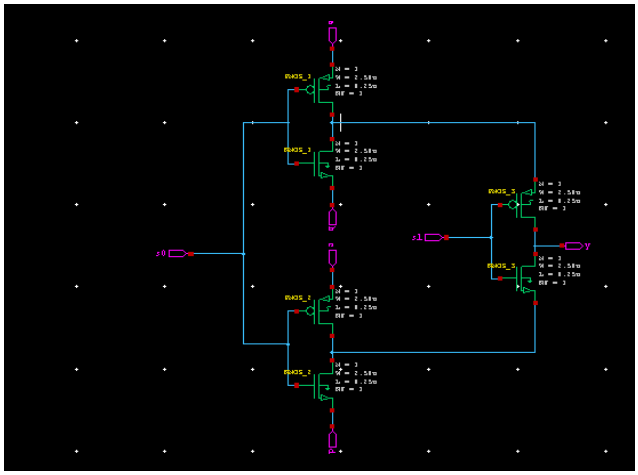

Fig 4: 4X1 mux using GDI

From fig we conclude that GDI technique uses less number of transistors resulting in less power dissipation as compared to CMOS.

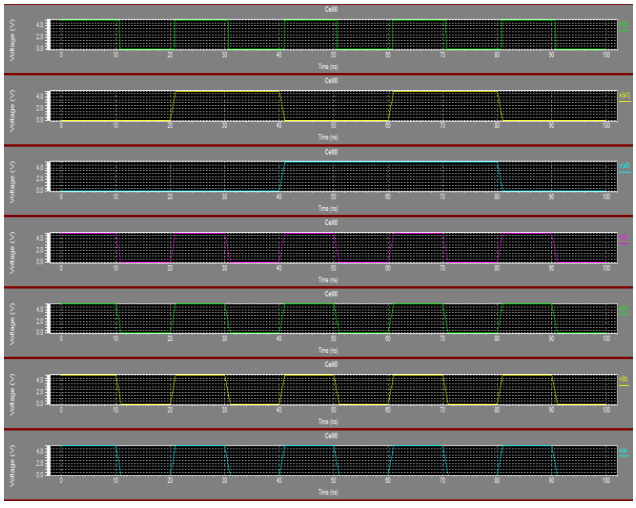

Fig: 5 GDI waveform

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3.3. Dual Pass Transistor Logic (DPTL)

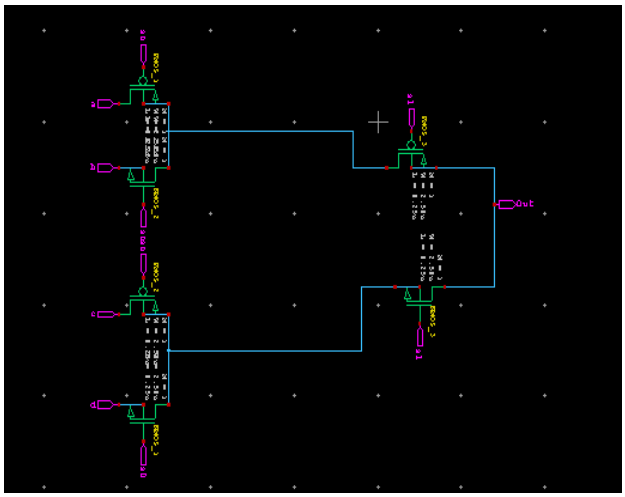

Fig 6: 4X1 mux using DPTL

From fig we can say that from this technique we get high speed as compared to other technique.

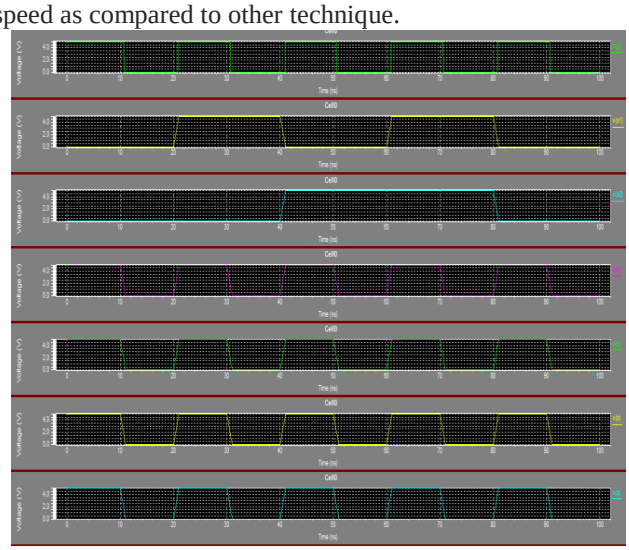

Fig: 7 DPTL waveform

3.4. Pass-Transistor Logic style (PT)

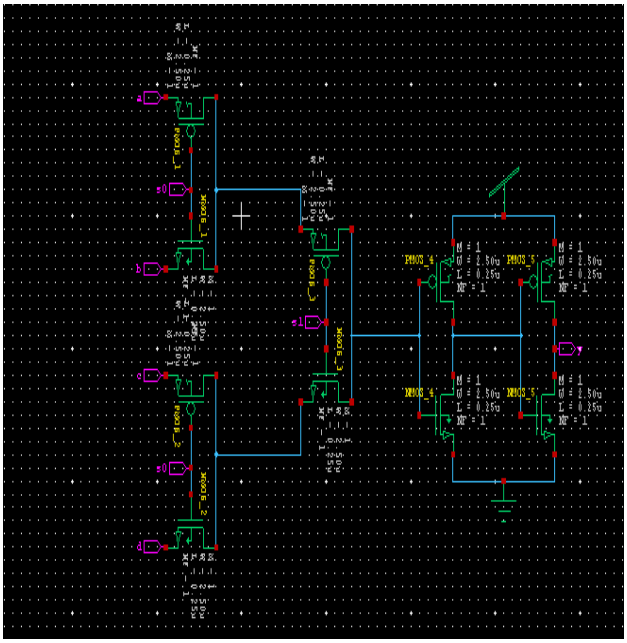

Fig 8: 4X1 mux using PTL

From fig we get high speed as compared to other techniques it is seen that from this technique.

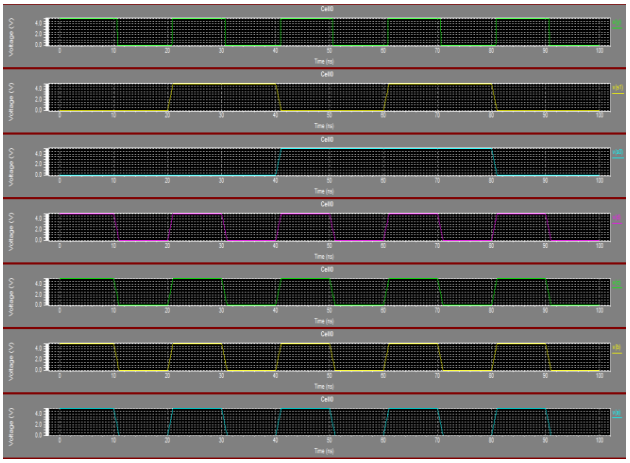

Fig: 9 PTL Waveform

3.5. Transmission gate (TG) logic

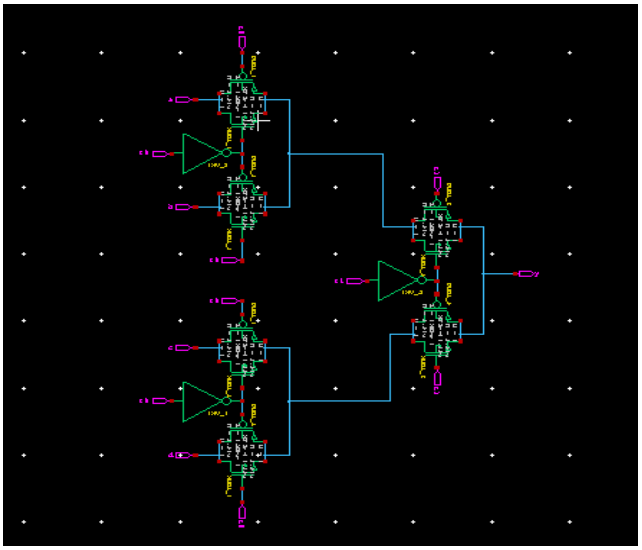

Fig 10: 4X1 mux using TG

From fig we get high speed with low power as compared to other techniques it is seen that from this technique

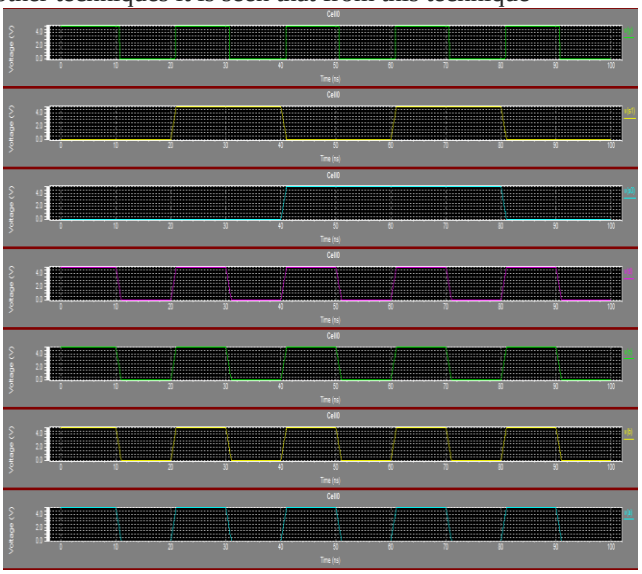

Fig: 11 TG Waveform

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IV. COMPARISION 0F VARIOUS DESIGN TECHNIQUES ON THE BASIS OF DESIGN METRICES

TABLE 2:

Sr. no	Technique	Transistor count	Speed	Power Dissipation	used Area
1	CMOS	26	HIGH	$10.511x10^{-8}$	MORE
2	GDI	6	LOW	$4.153 x10^{-8}$	LOW
3	DPTL	6	LOW	$8.907 x10^{-8}$	LOW
4	PT	10	HIGH	$8.657 x10^{-8}$	MORE
5	TG	14	HIGH	$5.158 x10^{-8}$	MORE

V. CONCLUSION

In this paper, the digital circuit 4X1 mux was implemented by different low power techniques namely CMOS, GDI, DPTL, PTL and Transmission Gate. The results were simulated using tanner EDA and comparison has been done for different parameters like power dissipation, speed, area and transistor count.

The results concluded that as compared to other proposed techniques, CMOS has more power dissipation and transistor count. These advantages of proposed techniques over CMOS make them more efficient and convenient to be used in digital circuits

REFERENCES

1. "Design And Simulation Of 4*1 Mux Based On Low Power Design Techniques"- volume 2 Issue 2 March-April 2015
2. "Design of Low power multiplexers using different Logics"- Vol.- 4, Issue – 2 pp 2229 – 6646
3. "low power cmos logic circuits" volume 2 Issue 2 481-520
4. "Top-down pass transistor logic design" IEEE J. Solid-State Circuits, vol. 31, pp 792–803, June1996.
5. "Low power CMOS digital design," IEEE J. Solid- State Circuits, vol 27, pp.473– 484, Apr. 1992.
6. "Low-power logic styles: CMOS versus pass- transistor logic" IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079{1090, Jul. 1997.
7. "Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic" in IJETT, 2013.
8. "Gate-diffusion input (GDI) – A technique for low power design of digital circuits: Analysis and characterization," in ISCAS, May 2002.
9. "design and implementation of low power 4:1 multiplexer using adiabatic logic"(IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.

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