



# Power Minimization Architecture for Multimodal Biometric System using Cadence

Manasa M.G, Gayathri S

*Abstract Physiological or behavioral characteristics of a person being identified or verified using biometric systems. The preprocessing block has the fir filter in which enhanced energy-efficiency has been obtained by introducing the low power architectures within it. The implementation of low power architectures in the fir filter part will further provide the optimization in the various parameters such as power, area and timing. Therefore, this will help us to do the biometrics process faster and efficient.*

**Keywords:** Multimodal biometrics, Low power architecture, Ear recognition.

## I. INTRODUCTION

The basis of every access control system is Identification. Three distinctive methods are used for authorizing identity. They are like cards, badges, keys, Information like user identity, password, Personal Identification Number. The first two method have weakness, which is inevitable. The identity of a person being directly plaid using biometric identification schemes.

Biometric identification schemes are disseminated into broad categories. These are:

Active biometrics: They are inherently invasive. They require a subject to chip in actively in both enrolling in the system and during consequent identification scheme.

Passive biometrics: Do not need a client's effective involvement and can be profitable without even a person knowing that they probed. Instances include voice recognition technologies, Iris recognition technologies, Facial recognition - truly passive and Ear recognition.

The current work employ both active biometry –Fingerprint and passive biometry – Ear for identification of a specific individual. Uni-modal biometric systems have a mixture of glitches such as, inter-class variations, noisy data, spoof attacks, obnoxious fault rates and delimited degree of autonomy. Multimodal biometrics signifies the fusion of two or more biometric modal qualities into a single object for detection. In the current work, ear and fingerprint are the two modalities considered for biometric systems.

## II. RELATED WORK:

[1]A robust and efficient ear biometric recognition scheme is proposed in [1] algorithm. The planned ear biometric system comprises of the subsequent phases: (i)

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Acquisition of ear images: (ii) Ear data withdrawal and regularization. (iii) Fuzzy filter is employed to eradicate the spikes completely and holes from the withdrawal ear region (iv) Canny edge detector is used to isolate the edge features from the ear data. (v) Feature matching and Recognition: using neural network algorithm.

The task of biometric recognition based on fingerprint is evaluated by using different classifiers in [2].they are 1.Neural Networks 2. Support Vector Machines configured with radial basis function 3. Optimum Path Forest 4. K-nearest neighbors and 5.Extreme Learning Machine.

Tentative grades conducted on an openly accessible database are listed. It is witnessed that the Support Vector Machine provokingly beat the further classifiers.

The Fingerprint Recognition system is based on using minutiae matcher method is presented in [3].The algorithm is examined precisely and consistently by using fingerprint images from diverse databases.

Personal identification is done by considering ear and fingerprint multimodal biometric system.to determine the ear features in [4] a novel performance-edge interaction point recognition is considered. Fingerprint themes are recognized by line based coupled component investigation and its feature vectors are constructed by using EIPD system. Mixture of features is carried out at the feature level and it is carried out through concatenation for features. Neural network based back transmission network is utilized for a distinctiveness authentication system.

An effortless and least time spending scheme for ear feature extraction using MATLAB as a processing tool is used in [5]. It includes following steps: Image acquisition, image preprocessing which includes cropping, greyscale conversion, enhancement and segmentation followed by feature extraction is done by canny edge detector.

[12] Personal identification is done by considering ear and fingerprint biometric data. An exclusive practice of edge collaboration point recognition is used to finalize the ear themes. Fusion at the feature level is carried out through nexus for features. Neural network based back transmission network is utilized for a distinctiveness authentication system.

[13]In many real time digital applications, power dissipation and hardware size are the major constraints. Numerical transformation called number separation with a shift and add decay scheme is presented in [7]. The speed of the system is increased by reducing the size of the hardware, power consumption and path delay. The designs are modeled using VHDL and implemented in Xilinx Spartan FPGA.

Validation of proposed work is done with respect to speed and area. Disintegration logic is employed with Baugh-Wooley algorithm to enhance the speed and to diminish the perilous path delay. In [14] a greater swiftness multiplier is planned and employed by means of decomposition logic and Baugh-Wooley algorithm. The outcome is compared with booth multiplier. An Architecture is developed and design is realized using XILINX ISE 12.3. [15] As technology is growing rapidly, researchers are continuously developing new multipliers with greater swiftness, low power utilization. To achieve speed improvements Baugh-Wooley Multiplication technique used for signed multiplication analysis is done based on LUT's and slices for related & unrelated logic are done

[10] Multiplier modules are common to many DSP applications. The quickest multipliers are parallel multipliers. Multipliers are selected and the selection is based on the criteria like regularity, high performance and low power consumption. The prime choice would be Booth multipliers. Booth multipliers support the operation for signed operands in 2's- complement. The next version of this multiplier algorithm accomplishes a major performance enhancement through radix-4 encoding.

[16] While designing a fast pace adder, factors such as area, delay and power are considered. The carry skip adder limits the time required for the propagation of carry in contrast to carry look ahead adder.

A carry skip adder (CSKA) arrangement has a greater pace, consumes least power in contrast with the conventional ones [17]. The pace augmentation is accomplished via nexus and incrimination methods to enhance the efficiency of the typical CSKA structure. As a substitute to multiplexer logic, the suggested structure has AND OR Invert - AOI and OR AND Invert - OAI complex gates for the skip logic. This results an improvement of 44% and 38% in the delay and energy respectively, compared with those of the Conventional-CSKA. Furthermore, the power delay product is the least among the various available structures, while its energy delay product is similar to the Kogge-Stone parallel prefix adder with noticeably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA disclose drop in the consumption of power in contrast to the most recent effort in this field while having a judiciously greater swiftness.

The performance of Carry skip adder using NMOS pass transistor logic configuration is presented in [18] and the logic we used in this paper is NMOS pass transistor the configuration of power dissipation, area, and delay. It is found that 50% decrement in interconnect length, area, and number of transistor count while using a pass transistor logic in comparison of 4-bit carry skip adder with a CMOS logic configuration. Reduction in power dissipation up to 9.87% delay up to 60% the parameter considered are transistor count is 35.2% is observed 180nm technology

Modified Booth Multiplier is practiced for signed multiplication in [19]. Baugh Wooley Multiplier is an added advantage for signed multiplication. It is not familiar due to dense in its assembly. The analysis is carried out using Cadence, with 180nm technology to calculate delay, area and energy. The results are better than the results Modified Booth Multiplier.

An ear recognition technique based on GLCM algorithm produced attractive and most acceptable results in contrast to ICP, PCA algorithms.

GLCM elucidates the texture of an image through a matrix formed by considering the number of occurrences of two pixels which are horizontally adjacent to each other in row and column and color features are extracted using hog descriptor.

For fingerprint identification minutiae features are extracted and classifier used is support vector machine. And also used some low power architectures in the multimodal system to provide the efficient performs in terms of the power consumption.

### III. METHODOLOGY

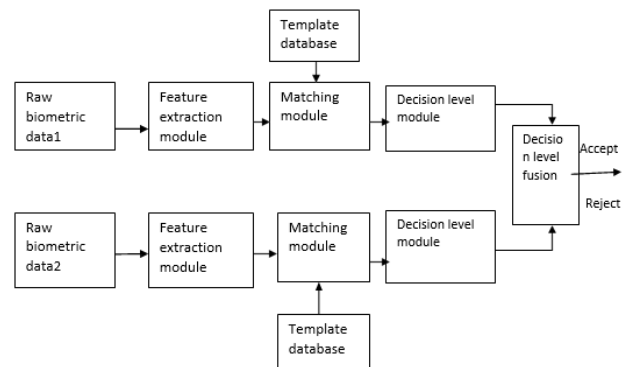


Fig1 Multimodal biometric system.

Fig1 shows the block diagram of multimodal biometric system. The person tenders data to the biometric system, then the processed data is coordinated in contrast to the associated template. Dissimilar feature sets are mined from numerous biometric modalities into a single feature vector that results feature level blending.

The results of the feature level extraction produces a template by comparing each input feature with the features available in the database.

The decision level fusion produces the results by data integration. The integrating of data occurs during each biometric system makes an independent decision for authentication of identity.

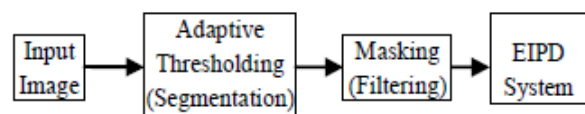


Fig 2 block diagram of preprocessing stage

Segmentation and masking methods are present in preprocessing block at the input image as in fig 2. Segmentation splits an image into its integral regions. The result of black and white image from a grayscale image is acquired through adaptive thresholding. After the preprocessing, thresholding T is decided by a series of reiterations, gray level values at every pixel is rounded up or rounded down

Masking is a type of spatial filtering wherein a specific limitation is set over the test image such that it filters out only the essential data and junks the rest.

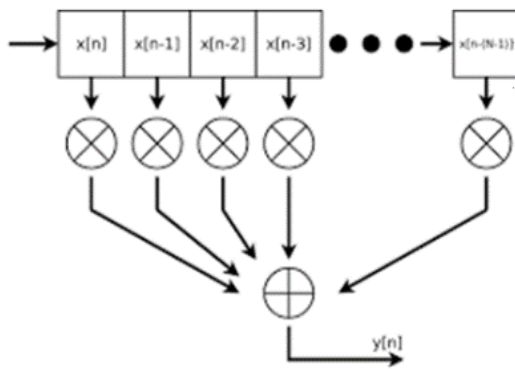
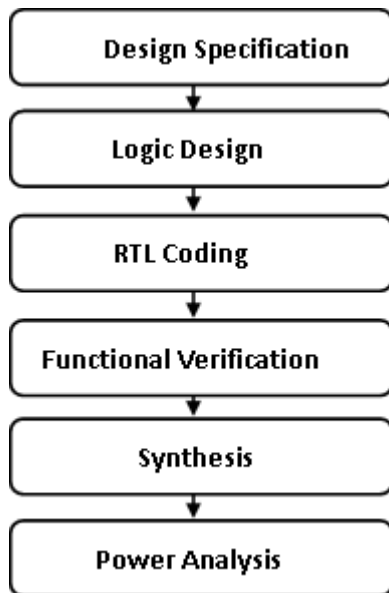


Fig 3 FIR FILTER

BAUGH-WOOLEY algorithm is used to reduce masking through FIR filter as shown in fig3. To boost the swiftness and to diminish the perilous path delay decomposition logic is used with BAUGH-WOOLEY algorithm.

The multiplier used in the fir filter majorly consists of adder blocks within it. So let us consider the ripple carry adder and carry skip adder for the efficient architecture in the filtering part of the preprocessing block in multimodal biometric system.



Four bit number can be added by cascading several full adder circuits in parallel. It is termed as a ripple carry adder because each carry bit becomes hooved into the next stage. In a ripple carry adder the sum and carryout bits of a half adder stage is invalid until the carry-in of that stage occurs. The reason for this is transmission delay within the logic circuit.

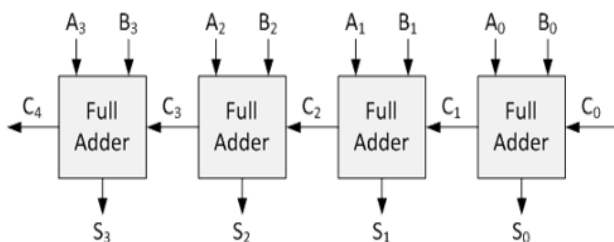


Fig 4 4 bit Ripple carry adder

The ultimate outcome of the ripple carry adder is efficient only after the mutual propagation delays of every part of full adder circuits inside it.

Compared to other adders a carry-skip adder forge ahead the delay of a ripple-carry adder with little effort

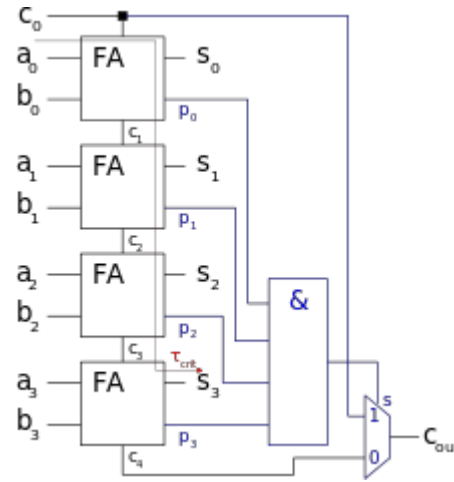


Fig 5 Carry skip adder

- A carry skip adder uses 2 signals Generate and propagate
- Propagate;  $P_i(A,B) = A_i + B_i$ .
- Generate;  $G_i(A,B) = A_i * B_i$ .
- G is the generate function- when both a and b are 1, there is a carry generated.
- P is the propagate function- when a is 1 it will propagate a carry in.
- When both inputs are 1, the G function generates a carry so either form of the p function work.

#### IV. IMPLEMENTATION

- 1. Design Specification:** Describe the functionality, interface, and the architecture of the digital design.
- 2. Logic Design:** Analyze the design's logic functionality, performance, to the given standards, and others specifications.
- 3. RTL coding:** Describe the logic either at Behavior/Dataflow/Structure/Switch level using HDLs: Verilog/VHD.
- 4. Functional Verification:** Run simulations to verify functionality using CAD tool.
- 5. Synthesis:** using RTL description Automatic generation of generic gate description is carried out. Logic optimization for different constraints such as Area, Performance & Power. Data path optimization, Power optimization
- 6. Power Analysis:** power consumption of the circuit is forecast by power analysis tool

- XPower Analyzertool
- Vectoredestination



V. ANALYSIS

The following are the work plans forthcoming for the next process.

The process of pulling out the features conducted to 30 people and the results are as follows:

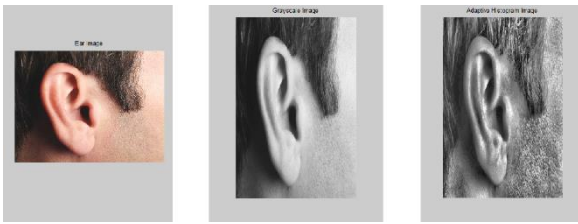


Fig 6: Ear feature extraction process

In the Fig 6, the feature extraction process is carried out to the lateral ear image, this is followed by the steps like image resizing, cropping, gray scale conversion and adaptive histogram equalization.

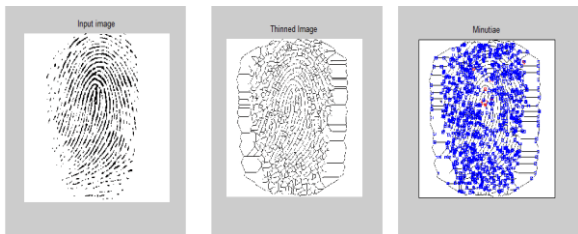


Fig 7: Feature extraction process for fingerprint

In the fig7, the feature extraction procedure is carried out to the fingerprint image, this is followed by the steps like image resizing, binarization, thinning and minutiae extraction.

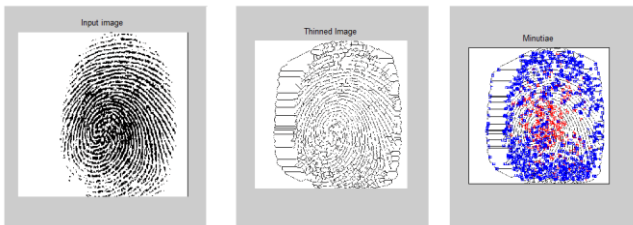


Fig 8: fingerprint feature extraction process

To authenticate the person biometric selected the ear sample of user1 is selected as shown in fig.9

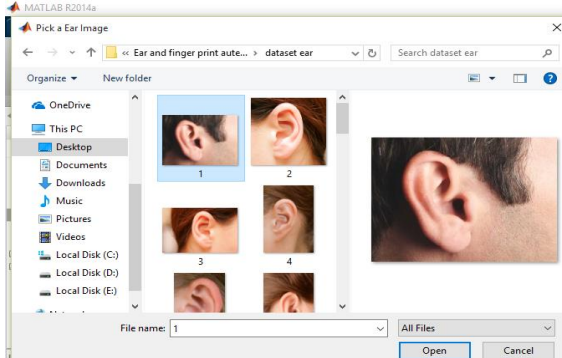


Fig 9: Selection of ear sample

To authenticate the person biometric the fingerprint sample of user1 is selected as shown in fig 10

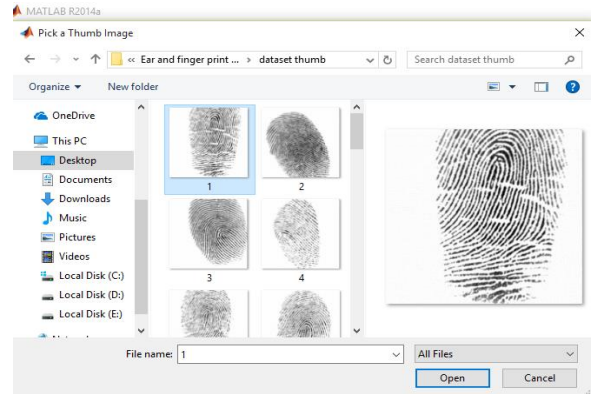


Fig 10: Selection of fingerprint sample

Since both the samples are of same individual, person gets authenticated.

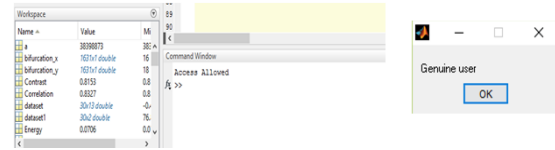


Fig 11: Result of the above selected samples

The ear sample of user2 is selected as shown in fig12

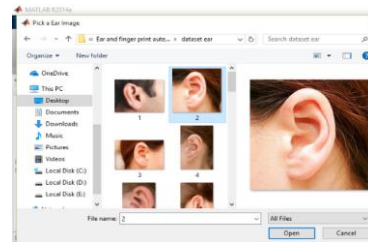


Fig 12: Selection of ear sample

The fingerprint sample of user1 is selected as shown in fig 13

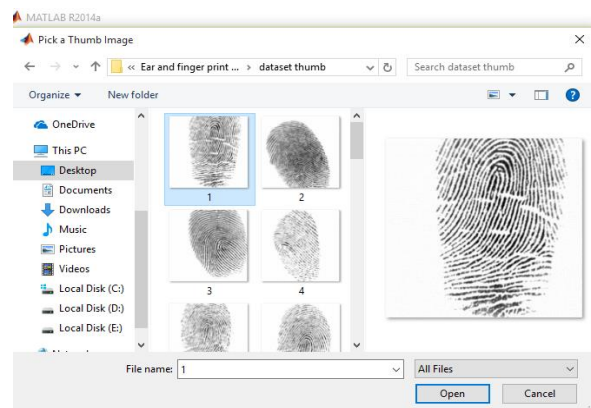


Fig 13: Selection of fingerprint sample

Since both the samples are of different individual the person is declared as an imposter.

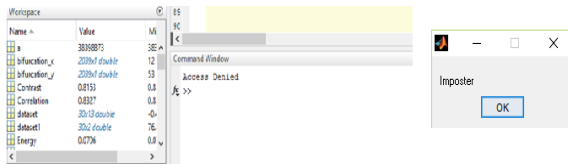


Fig 14: Result of above selected samples

**Parameter comparison 8 bit multiplier using CADENCE TOOL:**

1. Dynamic Power (nW)-less compared to existing multiplier is about 6.5%

The above result shows that the multiplier block in fir filter of the preprocessing block in multimodal system reduction of power, with same area with no change in the results of MBS.

**VI. CONCLUSION**

In this paper, low-power processor architecture for Multi modal biometric application has been generated, tested and verified using industry level customary ASIC design methodology. Delay and dynamic power of the improvised data-path architecture were verified. The proposed architecture has reduced percentage of the power and area to the existing architecture. Power minimization of data paths blocks present in the preprocessing blocks has been considered and reducing upto 6.5% of the power using synthesis tool.

Different blocks of Multimodal biometric system is considered in additional analysis which includes upcoming architecture. Application suggests that the proposed data-path architectural optimizations are distinctive & universal since they can be applied to any abstraction level in the design cycle and for any bit width.

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