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A Hybrid Self-Voltage Balanced Multilevel Inverter Topologies for Induction Motors

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Abstract: ***A hybrid structured asymmetric switching capacitor multilevel inverter (ASC-MLI) is suggested in this work. The notion behind presenting this topology is to reduce the device count and DC sources as compared with conventional MLI. The step by step operating mode of single phase ASC-MLI is presented and by doing slight modifications the same configuration is used in three phase utility application and electric drive. The proposed configurations utilize major benefits of self-voltage balancing capability of capacitor voltage, which is independent from different load type and modulations index. To generate the switching pulse for corresponding switches the multi-carrier based sinusoidal pulse width modulation (MCS-PWM) technique is used; in addition to this simulation result are obtained using MATLAB/Simulink 2016b software version. Simulation results of an induction motor drive connected as three phase load highlights good performance of 17-level MLI.***

Keywords: Renewable energy system, Asymmetric switch-capacitor multilevel inverter (ASC-MLI), Multi-carrier sinusoidal pulse width modulation (MCS-PWM), Total harmonic distortions (THD).

I. INTRODUCTION

As the need for electrical power grows across the world, it is expected that power electronics system (PES) will be used in 100 percent of all electrical energy industry, changing the face of the electrical engineering sector [1]. Dc-to-ac power conversion is most significant technology for setting up generation, transmission, distribution, and electrical power utilization at the ongoing scenario as the uses of renewable energy system (RES) increases rapidly. Multilevel Inverter (MLI) has been a key technology in variable frequency drives using various utility applications, active filters, locomotives, and RES. A high-capacity uninterruptible power supply improves electromagnetic compatibility and ensures desirable output voltage quality. [2,3,4]. Its wide application makes it a mature technology, since traditional converters only generate two levels of output voltage, $+V_{dc}$ and $-V_{dc}$, which contain a high amount of harmonic components and require the use of a filter to assure a sinusoidal waveform. However, due to switching losses and the necessity for high-rated components, traditional converters have some limitations when used at high voltage/power applications. [7]. The requirement of MLI are less switch loss, and reduced dv/dt stress are all advantages of MLI [5,6,9]. Several MLI circuit configurations are available which are capable of synthesizing multilevel waveforms. Three topologies, however have acquired the status of being 'classic or conventional' topology [8]. These topologies are Neutral Point Clamped (NPC) MLI, Flying Capacitor (FC) MLI & Cascaded H-bridge (CHB) MLI [10-16]. The downside with NPC MLI configuration is as the output voltage level increases, it requires additional clamping diodes and also alarms whenever there is an unequal voltage sharing among capacitor which are connected in series [10]. When using FCMLI, a high number of storage capacitors are required to increase the amount and quality of output voltage as the stages to get desired waveform [11-12]. In CHB MLI configuration, no flying capacitor & clamping diodes are used; the only limitations with this configuration is that it requires isolated dc source as the output voltage level increases. As a result, a large range of MLI topologies and control schemes have been suggested in recent decades to reduce switched device count (RSDC) by using varying ratings of unidirectional and bidirectional switches [13-17]. Few of them are discussed here briefly. In [13-15], the MLIs having symmetrical topology has taken over, as they have less diversity in DC voltage source which results in low cost, but major concern with them is their modularity. In [16] a new configuration is presented which further is improved in [17], the primary disadvantage of this setup is that the suggested algorithm cannot achieve all of the stages (additive and subtractive). According to existing literature, the majority of reported MLI topologies in recent years have been achieving high output voltage levels with minimal numbers of switches. However, there has been a lot of tradeoff in terms of modularity, bidirectional switch simplicity, DC source variety, voltage stress against switch durability, and losses. This paper focuses on ASC-MLI topology which uses hexagonal switch cell [HSC] [11]. Using eight controlled switches, the suggested architecture can create 17 levels of output voltage. It provides dependable operation with decreased voltage stress across the switches due to its modular construction. Because the design has an inherent capacity of balancing capacitor voltage, it decreases DC source diversifications.

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II. PROPOSED MLI TOPOLOGIES

2.1 Proposed topology – I:

In the proposed work, a new configuration based on hybridized asymmetrical switched capacitor MLI is proposed, which is an extension of its basic unit [11]. The hybridized proposed topology is illustrated in fig 1, which is switched-capacitor based multilevel inverter (SCMLI), and requires two unequal dc voltage source (V_{SL} & V_{SR}), six bidirectional-conducting-unidirectional-blocking (BCUB) power switch, two bidirectional-conducting-bidirectional blocking (BCBB) power switches and two capacitor. Table 1 shows the generalized mathematical equation for asymmetrical operation and the DC value sources.

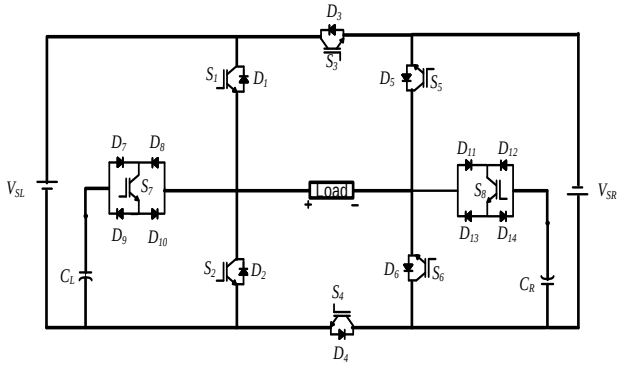

Fig. 1 Configuration of the proposed topology

Table 1. Realizations of Different Level of Proposed Topology

Value of DC source	Number of output levels
V_{SL1} = initial	$4x\left[\sum_{m=1}^{n}\frac{(V_{SLm}+V_{SRm})}{V_{SL1}}\right]+1$
$V_{SR1} = 3xV_{SL1}$	
$V_{SLn} = 4x[\sum_{m=1}^{n-1}(V_{SLm}+V_{SRm})] + V_{SL1}$	
$V_{SRn} = 2x[V_{SLn} + (\sum_{m=1}^{n-1}(V_{SLn}+V_{SRn}))] + V_{SL1}$	

*n = number of cell

To generate all possible levels (i.e. positive and negative) for the proposed configurations, the magnitude of voltage (V_{SL}: V_{SR}) should be (2:6) obtained from table 1. As indicated in Table 2, states 1 to 8 of the proposed MLI's output voltage waveform have positive levels, state 9 has zero levels, and states 10 to 17 have negative levels. The '1' state condition represents the switch in the 'ON' state, whereas the '0' state condition represents the switch in the 'OFF' state.

Table 2. Switching table for 17-Level Inverter Topology

State	Output voltage level	Switching scheme								Conducting Diodes
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	$V_{SL}+V_{SR}$	1	0	0	1	1	0	0	0	-----
2	$V_{CL}+V_{SR}$	0	0	0	1	1	0	1	0	D_7, D_{10}
3	V_{SR}	0	0	0	1	1	0	0	0	D_2
4	$V_{SL}+V_{CR}$	1	0	0	1	0	0	0	1	D_{11}, D_{14}
5	$V_{CL}+V_{CR}$	0	0	0	1	0	0	1	1	D_7, D_{10},D_{11}, D_{14}
6	V_{CR}	0	0	0	1	0	0	0	1	D_2,D_{11},D_{14}
7	V_{SL}	1	0	0	1	0	0	0	0	D_6
8	V_{CL}	0	0	0	1	0	0	1	0	D_7,D_6,D_{10}
9	0V	0	0	0	1	0	1	0	0	D_2
10	$-(V_{SL}-V_{CL})$	0	0	1	0	0	0	1	0	D_5,D_8,D_9
11	$-(V_{SL})$	0	1	1	0	0	0	0	0	D_5
12	$-(V_{SR}-V_{CR})$	0	0	1	0	0	0	0	1	D_1,D_{11},D_{14}
13	$-(V_{SL}+V_{SR}-V_{CL}-V_{CR})$	0	0	1	0	0	0	1	1	D_8,D_9,D_{12}, D_{13},
14	$-(V_{SL}+V_{SR}-V_{CR})$	0	1	1	0	0	0	0	1	D_{12},D_{13}
15	$-(V_{SR})$	0	0	1	0	0	1	0	0	D_1
16	$-(V_{SL}+V_{SR}-V_{CL})$	0	0	1	0	0	1	1	0	D_8,D_9
17	$-(V_{SL}+V_{SR})$	0	1	1	0	0	1	0	0	-----

OPERATING MODE OF PROPOSED TOPOLOGY - I

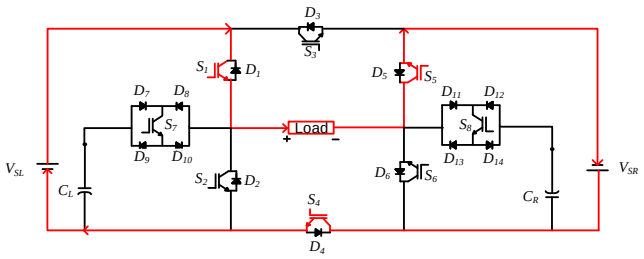

Fig (I) $+(V_{SL}+V_{SR})$ (Level +8)

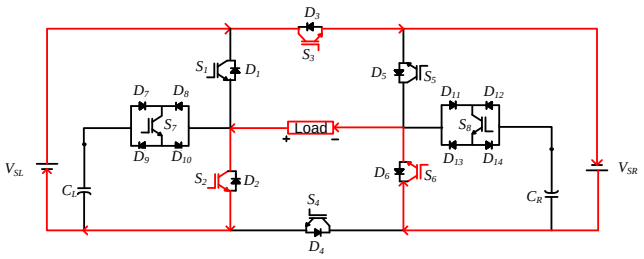

Fig (II) $-(V_{SL}+V_{SR})$ (Level -8)

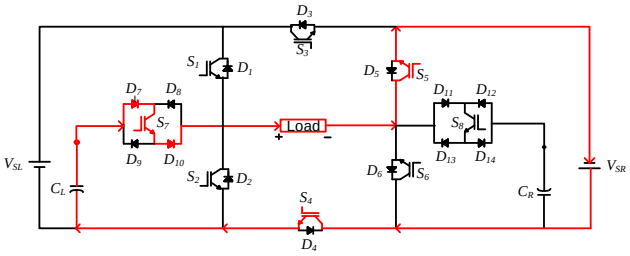

Fig (III) $+(V_{CL}+V_{SR})$ (Level +7)

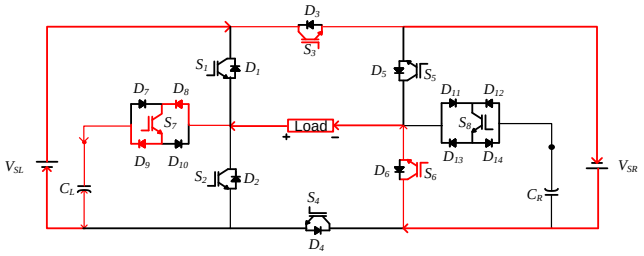

Fig (IV) $-(V_{SL}+V_{SR}-V_{CL})$ (Level -7)

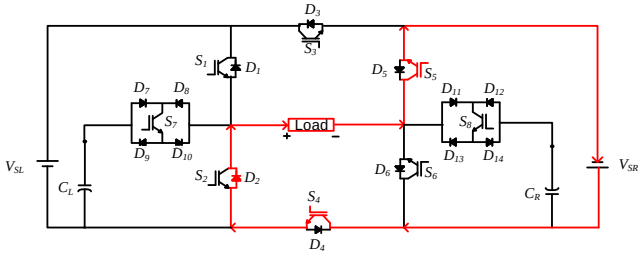

Fig (V) $+(V_{SR})$ (Level +6)

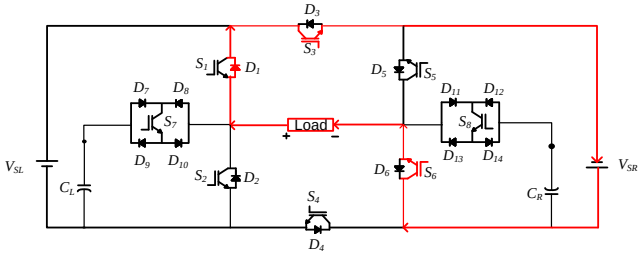

Fig (VI) $-(V_{SR})$ (Level -6)

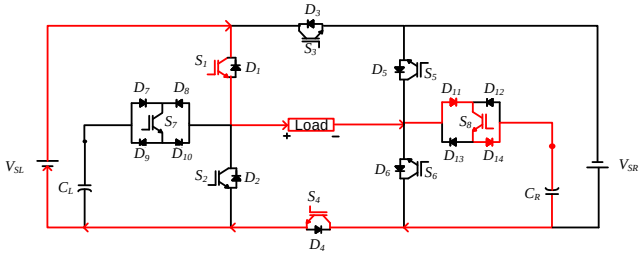

Fig (VII) $+(V_{SL}+V_{CR})$ (Level +5)

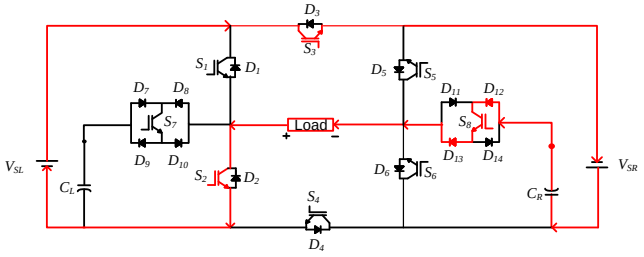

Fig (VIII) $-(V_{SL}+V_{SR}-V_{CR})$ (Level -5)

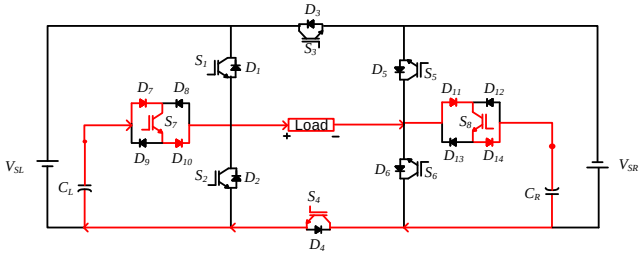

Fig (IX) $+(V_{CL}+V_{CR})$ (Level +4)

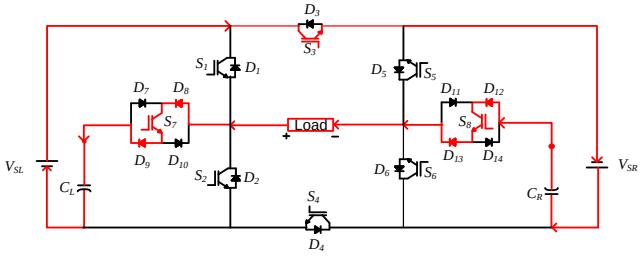

Fig (X) $-(V_{SL}+V_{SR}-V_{CL}-V_{CR})$ (Level -4)

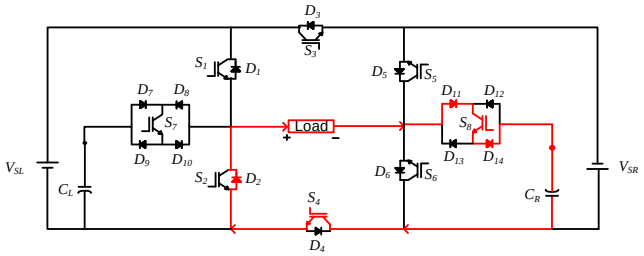

Fig (XI) +(V_{CR}) (Level +3)

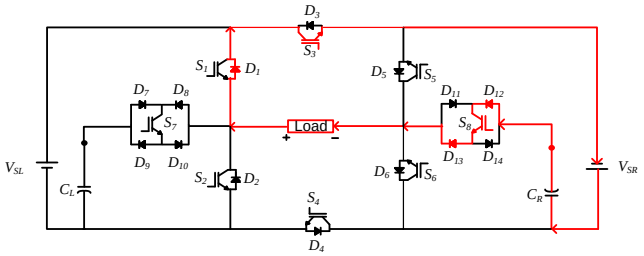

Fig (XII) -(V_{SR}-V_{CR}) (Level -3)

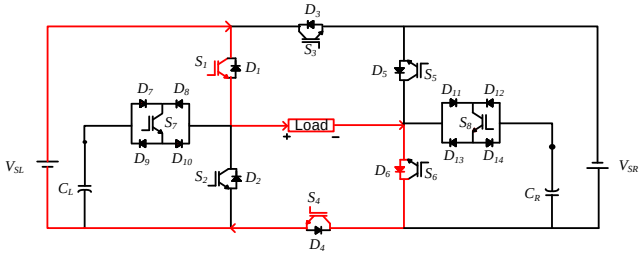

Fig (XIII) +(V_{SL}) (Level +2)

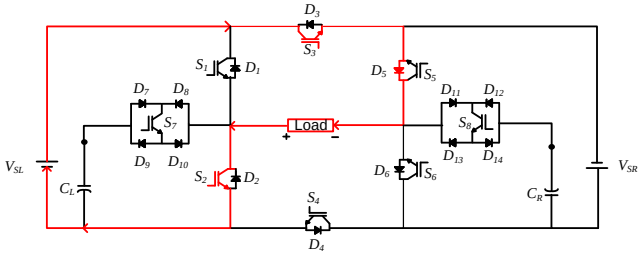

Fig (XIV) -(V_{SL}) (Level -2)

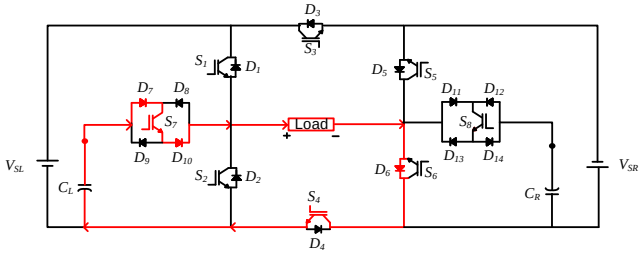

Fig (XV) +(V_{CL}) (Level +1)

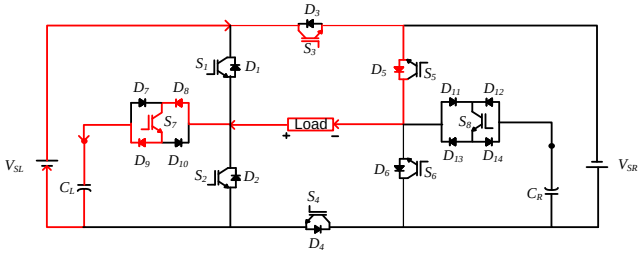

Fig (XVI) -(V_{SL}-V_{CL}) (Level -1)

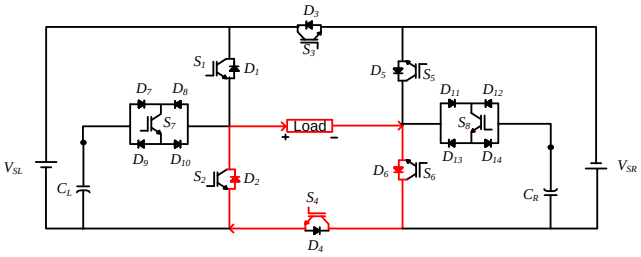

Fig (XVII) +(0 V) (Level 0)

Fig. 2 shows sub figs. (I-XVII) which are the distinct mode of operations (i.e. current flow direction) for the proposed topology for 17-levels output.

2.2 Proposed topology –II:

The topology I is used for the single phase operations, by doing slightly modifications it can be further developed to use in the three phase MLI applications. In the topology shown in fig. 3, three individual cells of topology I can be used and in their output, three phase load is connected.

Its switching signal is generated in such a manner that, by keeping their carrier signal same and making 120^0 phase shift in their reference signal.

III. MODULATING SCHEME

In both the topologies I & II, the operations of power switches are regulated by producing correct gate signals, which is done using a suitable MCS-PWM approach (i.e. alternating phase opposition disposition (APOD) pulse shift technique). The switching frequency of the carrier signal is kept at 5 KHz, while the frequency of the reference signal is retained at 50 Hz. In the MCS-PWM approach, an appropriate logical operation is employed between the carrier and reference signal to create desired pulses, which are then supplied to the power switch's corresponding driver circuit, which amplifies the amplitude of the generated pulses to activate the respective switch. [17]. To create ‘m' number of output levels, the MCS-PWM technique requires (‘m-1') carrier signal. Figure 4 depicts the fundamental structure that is employed in the 17-level MLI modifying schemes.

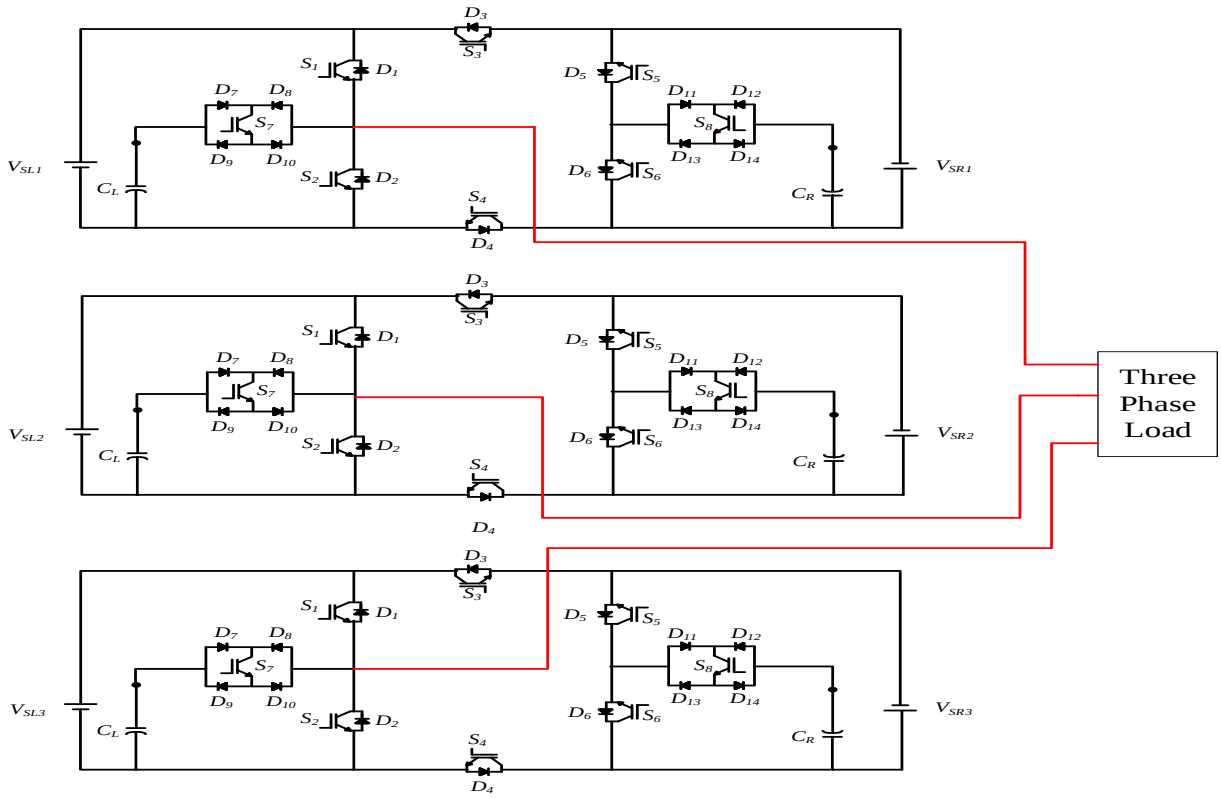

Fig. 3 Three phase connection of proposed topology II

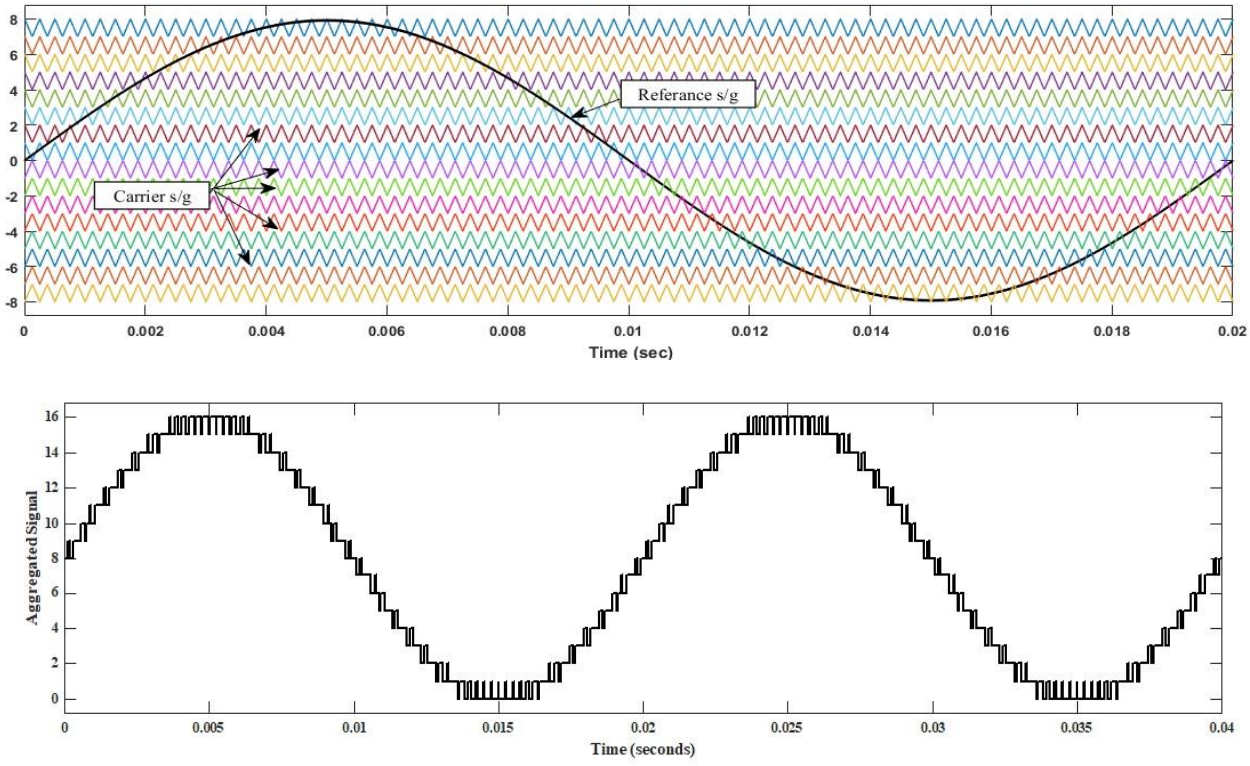

Fig. 4 Modulating Strategies for the 17-level MLI

IV. SIMULATION RESULTS

The simulation was carried out using MATLAB/Simulink to assess the performance of the proposed configuration. The simulation parameter for three phase MLI are as follows, V_{SL} = 30V, V_{SR} = 90V, balancing capacitor C = 1200µF each, load resistance R = 80Ω, load inductance L = 200mH, modulating index (m) is 0.98 and switching frequency is 5 KHz. Their phase voltage and line voltage are shown in fig. 5 & 6 respectively and FFT analysis in MATLAB/Simulink 2016b is generally applied to determine total harmonic distortion as shown in fig. 7.

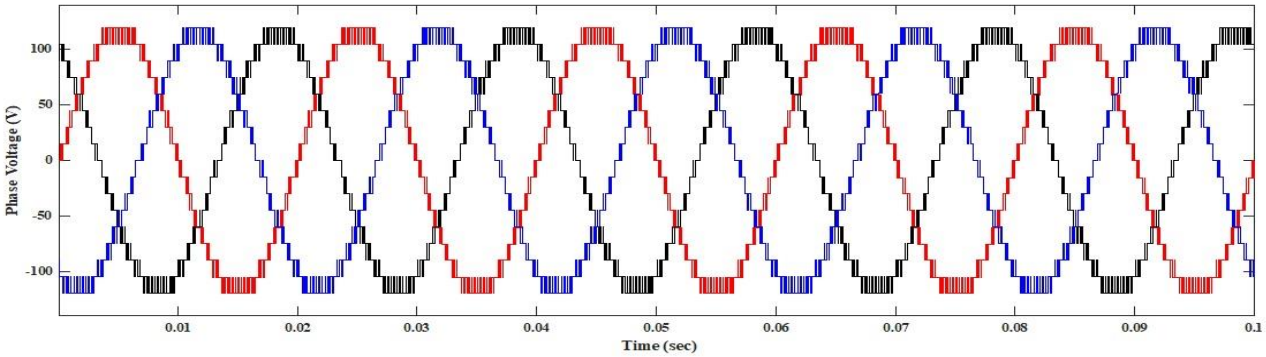

Fig. 5 Phase output voltage of 17-level MLI with RL load

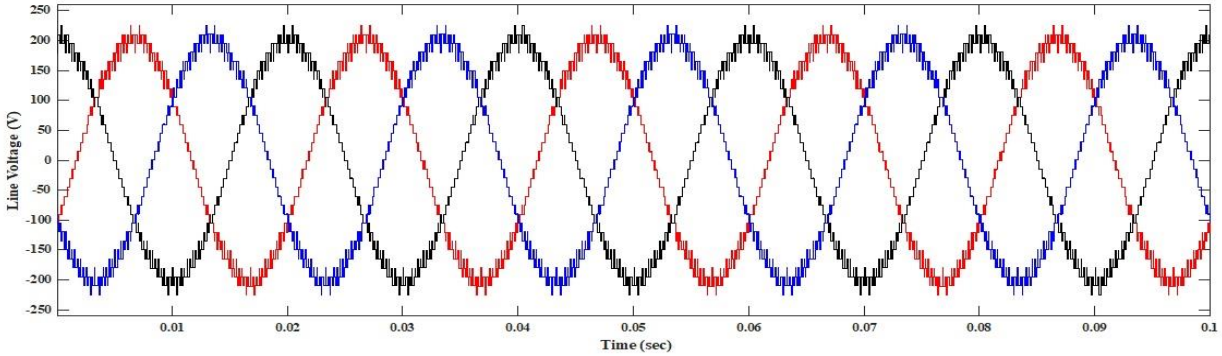

Fig. 6 Line voltage of 17-level MLI with RL load

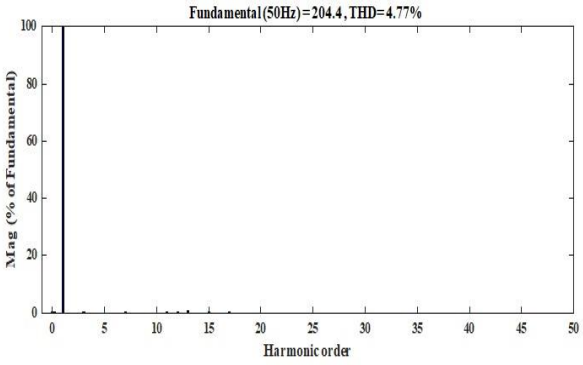

Fig. 7 Harmonic component of output voltage spectrum

Further to analysis the performance characteristics of an Induction Motor Drive such as speed, torque and stator current along with its line voltage and phase current, an induction motor drive is connected as a three phase load in the proposed three phase multilevel inverter configurations. The corresponding results are displayed by using MATLAB/simulations software. The simulation results of three phase line current and phase voltages of an induction motor drive are depicted in Figures 8 and 9, respectively. Figures 10, 11, and 12 represent the simulation results of induction motor speed, torque and stator current respectively.

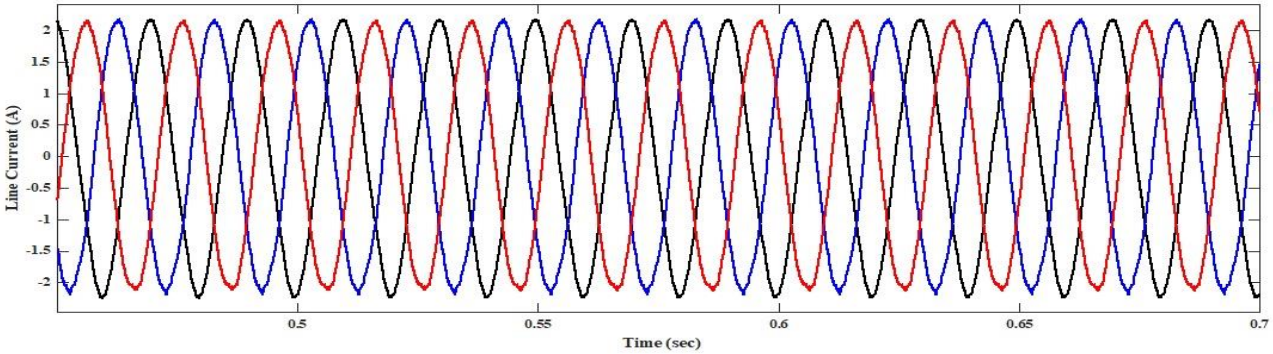

Fig. 8 Output current of 17-level MLI with induction motor as load

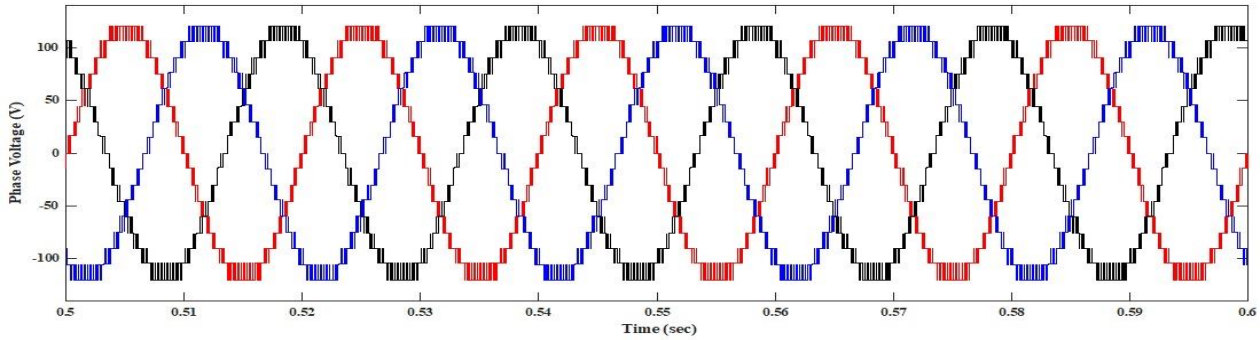

Fig. 9 Phase output voltage of 17-level MLI with induction motor as a load

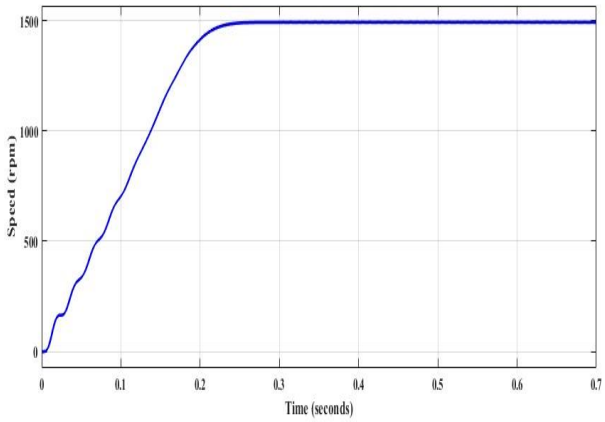

Fig. 10 Motor speed

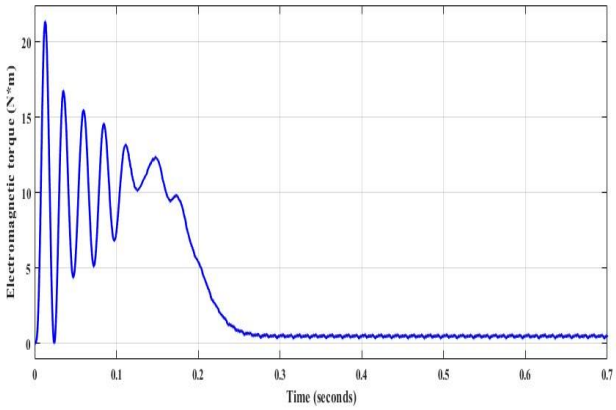

Fig. 11 Motor torque

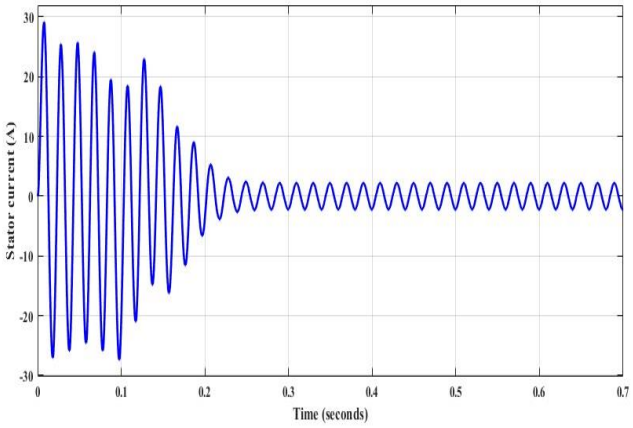

Fig. 12 Stator current

V. CONCLUSION

This work presents a new version of hybridized asymmetric switched-capacitor multilevel inverter (ASC-MLI) topology with reduced number of device counts. Proposed inverter uses switched capacitors which have inherent self-voltage balancing capabilities and suitable for low-voltage, high- current power and renewable energy applications. The PIV of all the power semiconductor switches are substantially lower than the operational voltage for all the modulation index ranges. Simulation results of the proposed configurations were successfully simulated and examine for 17-level invert which can produce all positive and negative levels with high quality of output voltage waveforms with minimum harmonics. Simulation results of an induction motor drive as a three phase load are also obtained to further validate a reasonable performance of 17-level inverter.

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